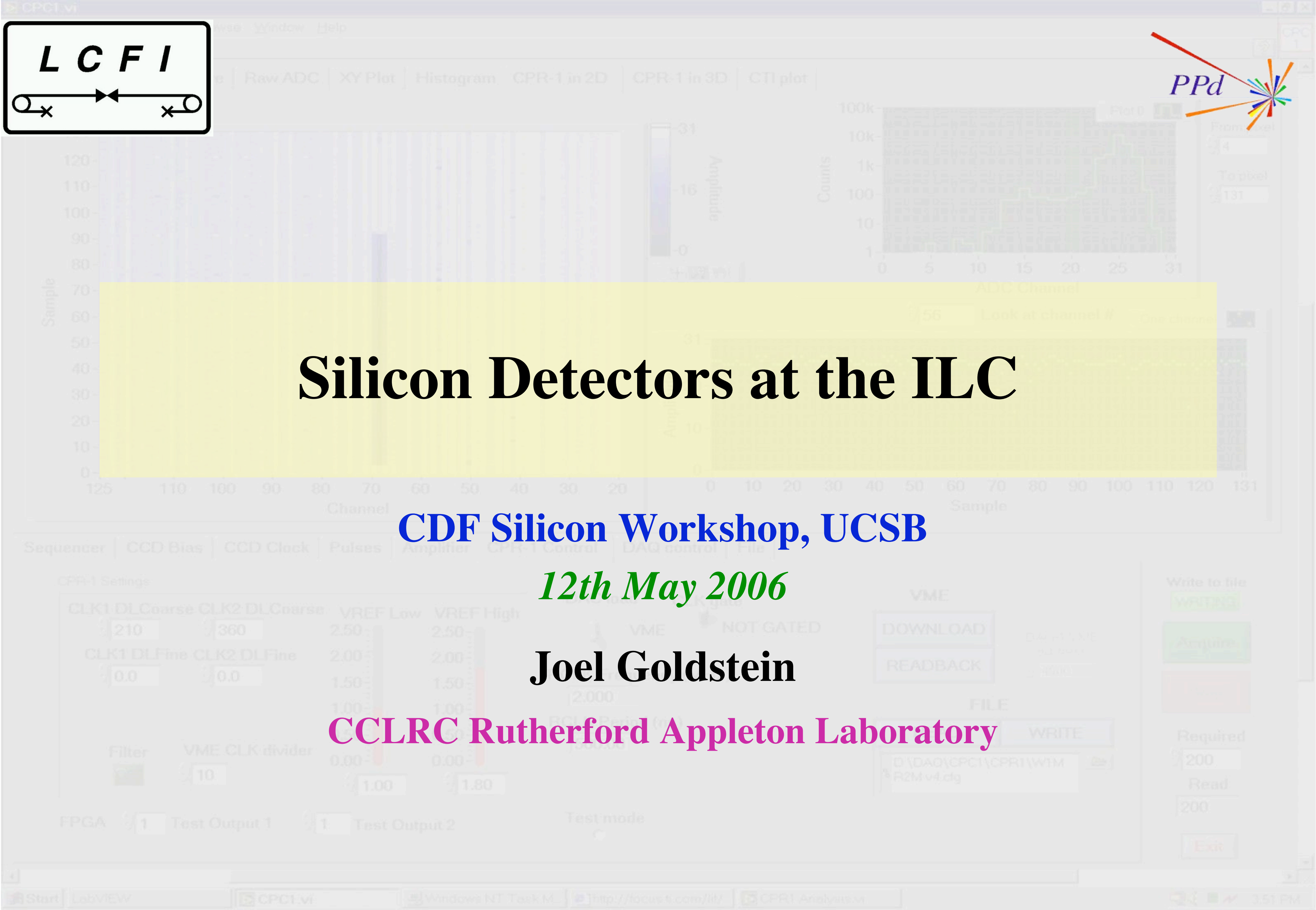


Silicon Detectors at the ILC

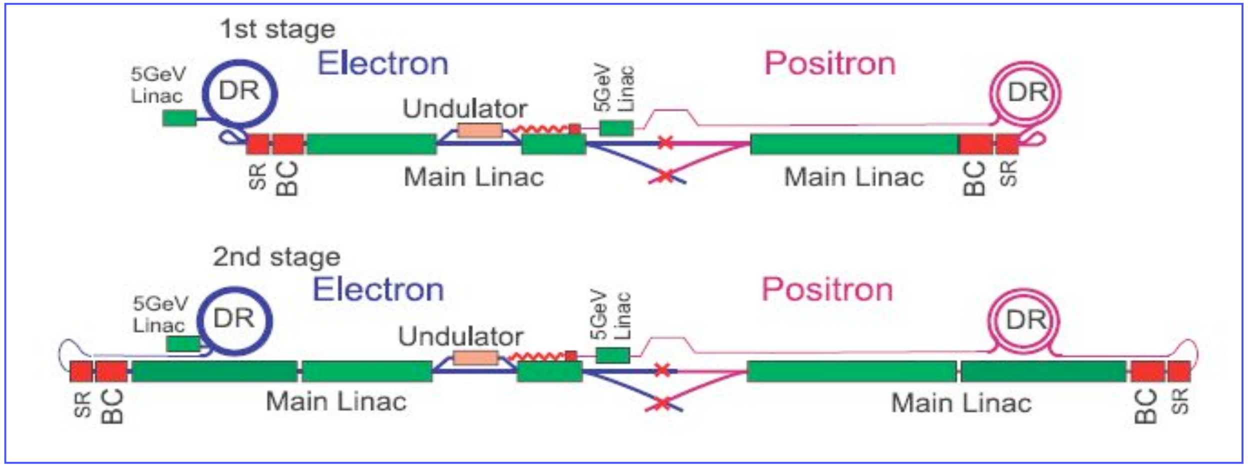
CDF Silicon Workshop, UCSB

12th May 2006

Joel Goldstein

CCLRC Rutherford Appleton Laboratory

The International Linear Collider



500 GeV e^+e^- Collider

- Upgrade to 1 TeV
- Superconducting RF
- Start in ~2015

- Low interaction rate
  - High p_t physics ~ 0.5 Hz
- Low backgrounds
- Low radiation
  - 10s of kRads per year

- Precision measurements
  - Build “dream” detector
  - No need for a trigger

Physics Benchmarks

Detector design driven by physics requirements

Limited by cost, real estate, technology….

- Calorimetry:
  - Separate hadronic *W*s and *Z*s (e.g. *ZZH*)
  - Jet energy: $\sigma_E \leq 30\%/\sqrt{E}$
- Tracking
  - Higgs recoil mass $HZ \rightarrow \mu\mu$
  - Momentum resolution $\sigma_{p_T}/p_T^2 < 5 \times 10^{-5}\ \mathrm{GeV}^{-1}$
- Vertexing
  - Higgs branching ratios, quark A_{FB}
  - Full 3D standalone reconstruction
  - $\sigma_{IP} \approx 5 \oplus 10/(p \sin^{3/2}\theta)\ \mu\mathrm{m}$

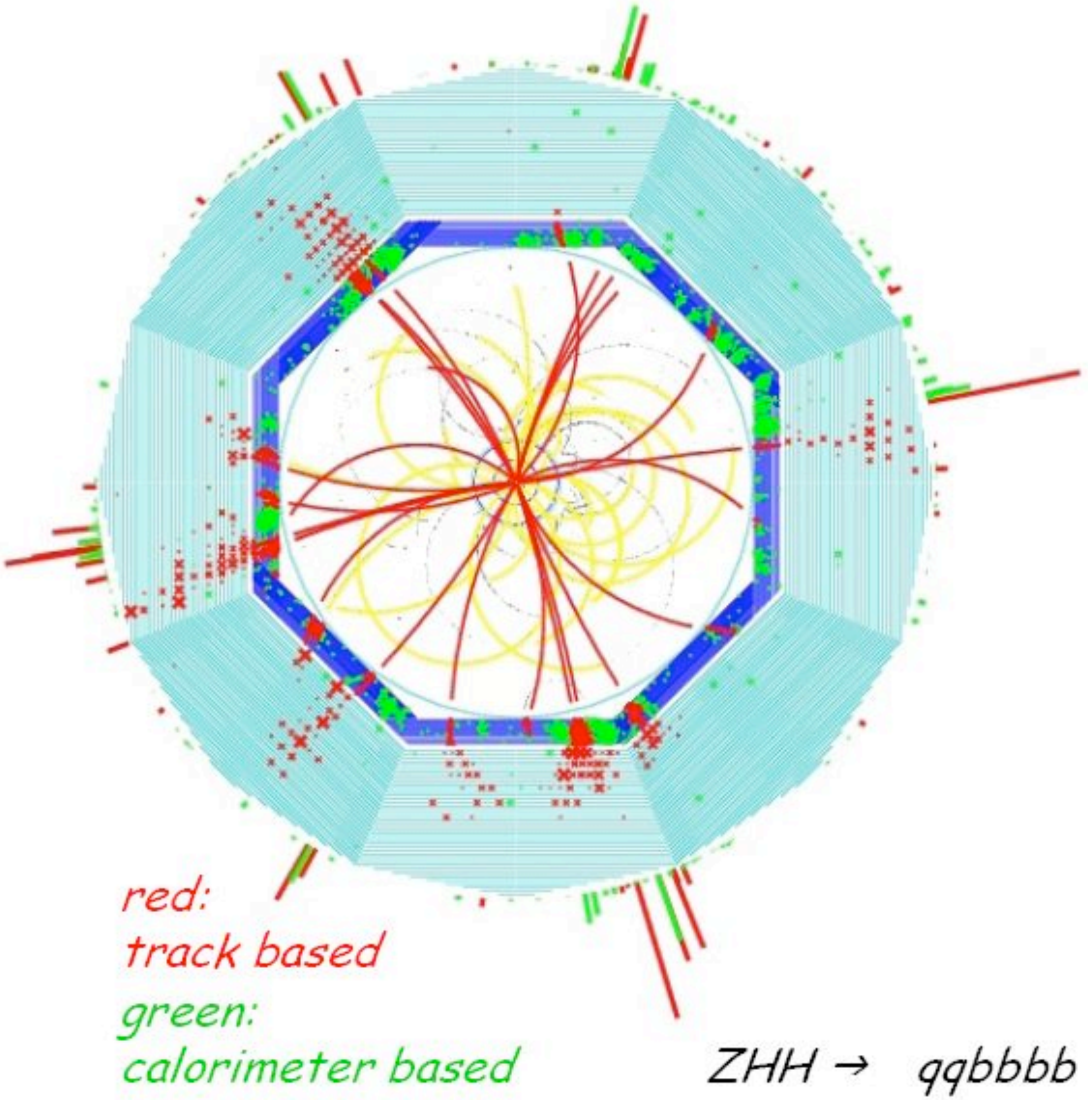
Particle Flow Algorithm

Jet $\sigma_E \leq 30\%/\sqrt{E}$:

1. **Separate energy deposits from individual particles**
2. **Identify particles**
3. **Use optimum method for each particle**

⇒ Calorimeter must have

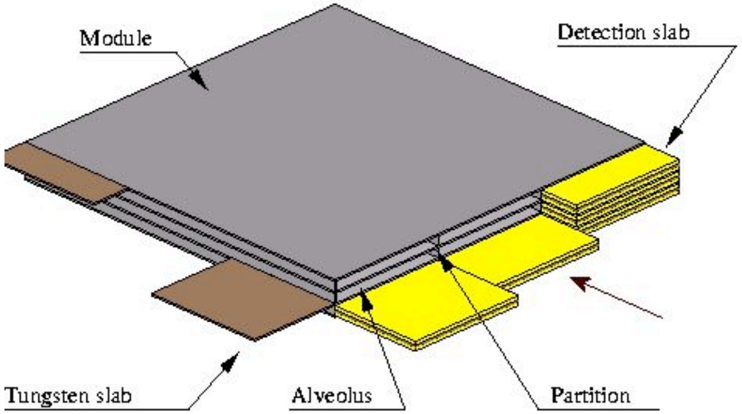
- ***High granularity***
- ***Small Moliere radius***

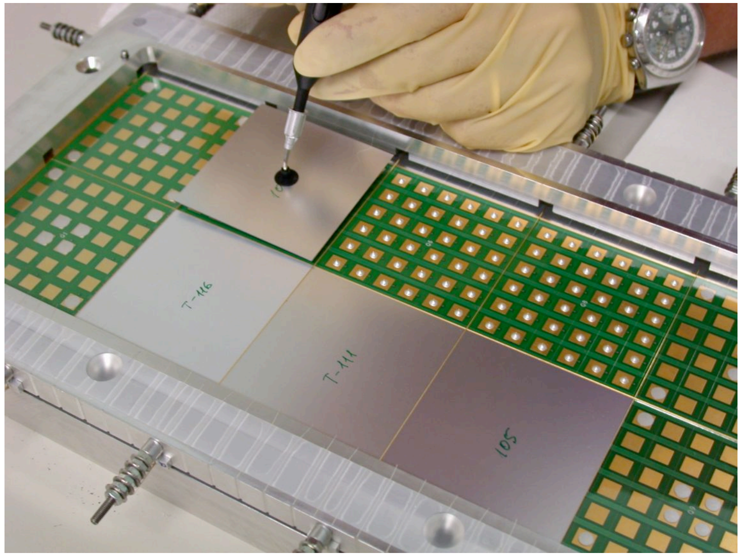


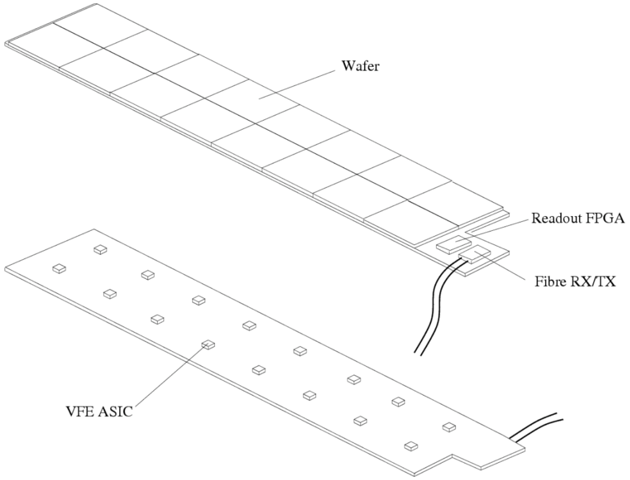
ILC Calorimetry

- Si-W sampling calorimeter
  - Extremely expensive
  - Probably only ECAL

    (Pb-scintillator HAD)
- 40 layers of 10×10 mm^2 pads



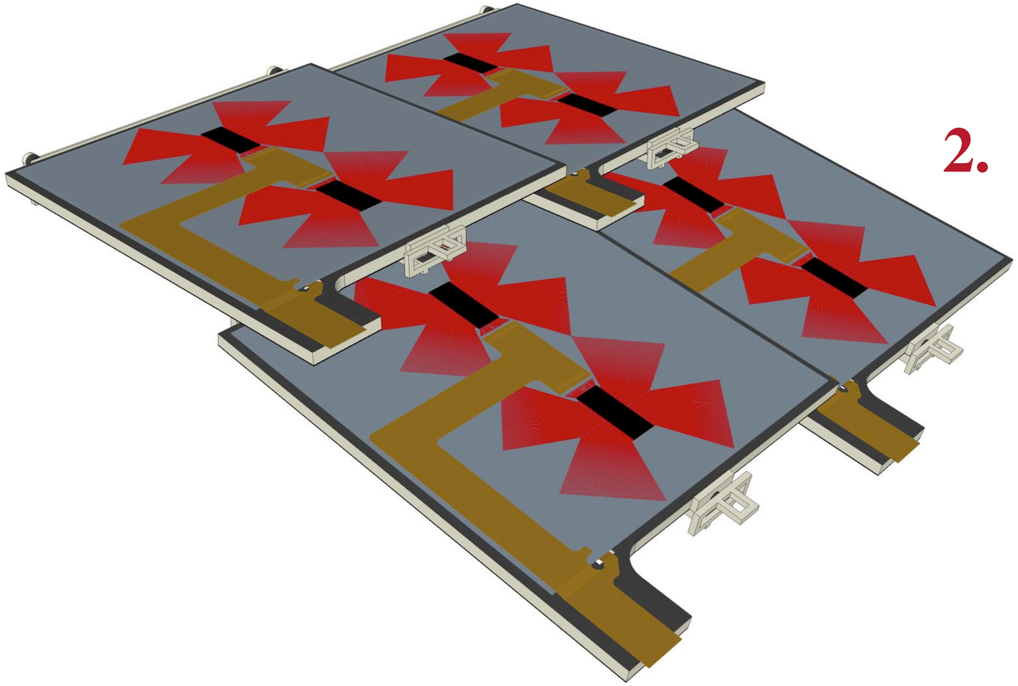




- 50×50 μm^2 digital pixels an option

ILC Tracker

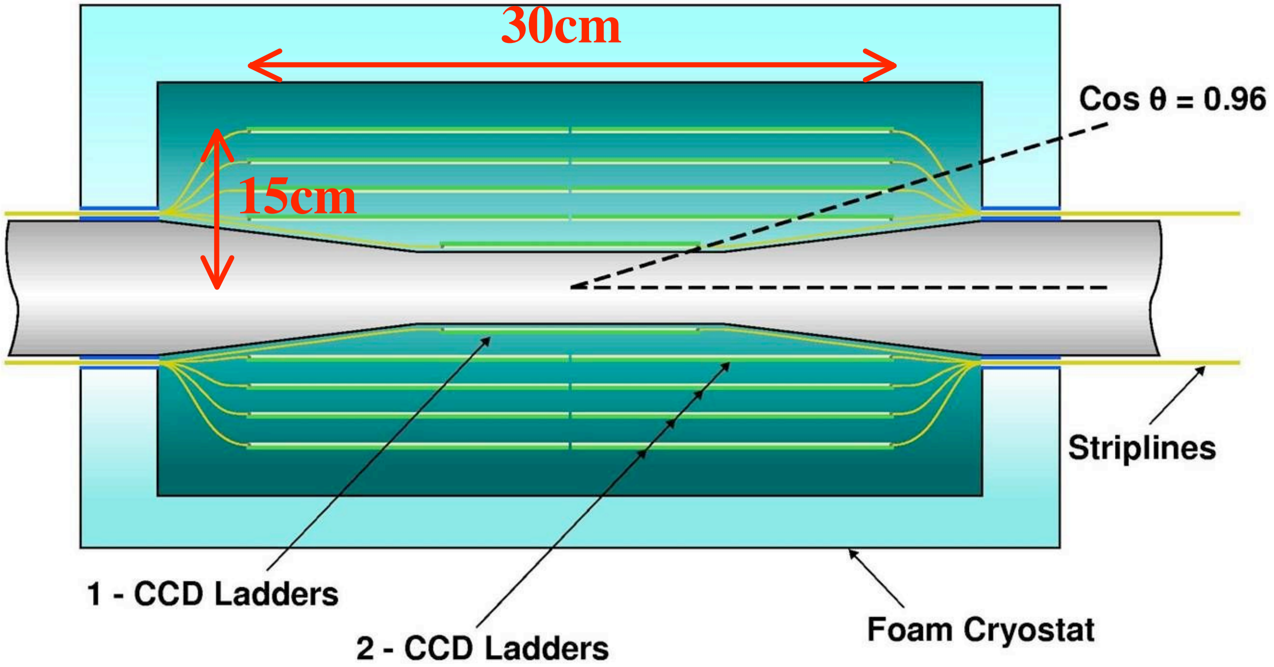
Momentum resolution: $\sigma_{p_T}/p_T^2 < 5\times 10^{-5}\ \mathrm{GeV}^{-1} \sim \sigma_{\mathrm{hit}}/BR^2$



Options:

1. Large TPC in 3–4T field
   - Silicon strips intermediate/forward
2. Smaller silicon tracker in 5T
   - 5+ layer strip detector
   - Probably axial only
   - ~1% X_0 per layer
     1. *Short modules* *(LHC)*
     2. *Long modules* *(CDF)*

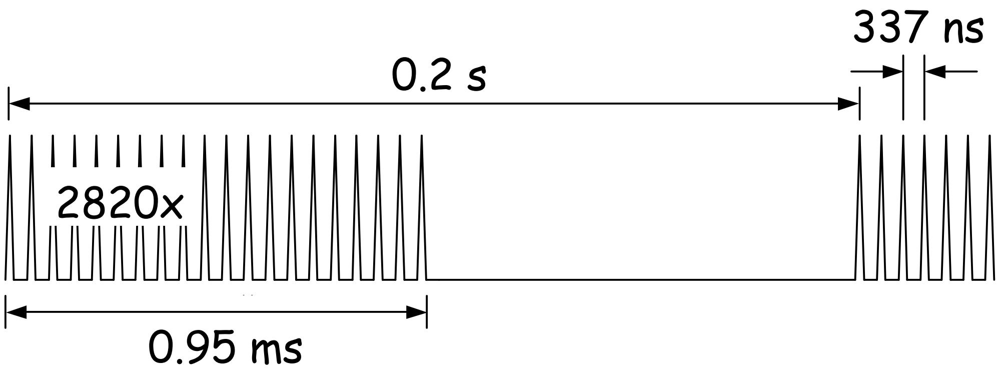
ILC Vertex Detector



- 800 Mchannels of 20×20 μm pixels in 5 layers
- Challenges:
  - "Beamstrahlung": 0.03 hits mm^{-2} / bunch
  - Material budget (~0.1% X_0 per layer)

Sensors: The Challenge

Beam Time Structure:



What readout speed is needed?

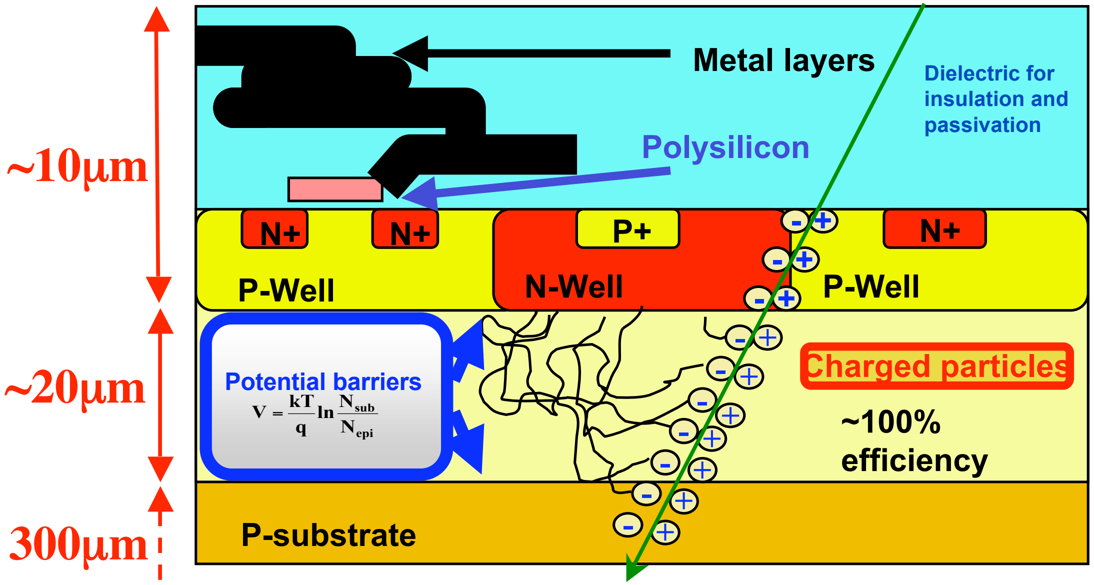
- Inner layer 1.6 MPixel sensors
- Once per bunch = 300ns per frame : *too fast*
- Once per train ~200 hits/mm^2 : *too slow*
- 10 hits/mm^2 => 50μs per frame: just right

(Fastest commercial imaging ~ 1 ms/MPixel)

Power dissipation – gas volume cooling

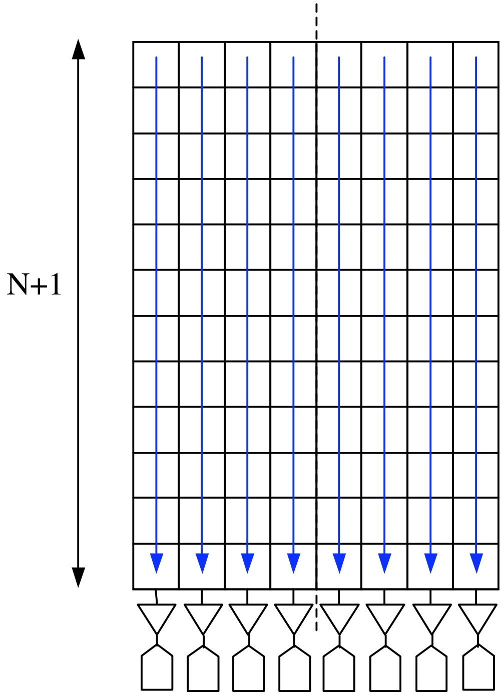
Silicon Pixel Detectors

- Read out during train:
  - Monolithic Active Pixels
  - CCDs
- Read samples after train:
  - MAPs
  - ISIS
- Other options:
  - Fine pixels (~1µm^2)
  - Time-stamping
- *All commercial products with thin active layer*

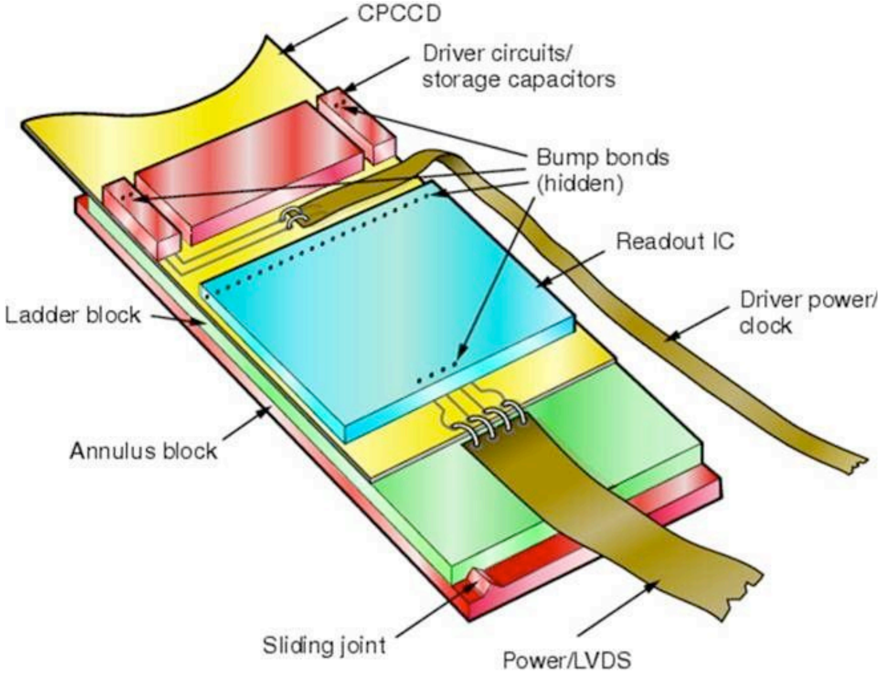


Column Parallel CCD

- Separate amplifier and readout for each column
- 50 MHz clock rate



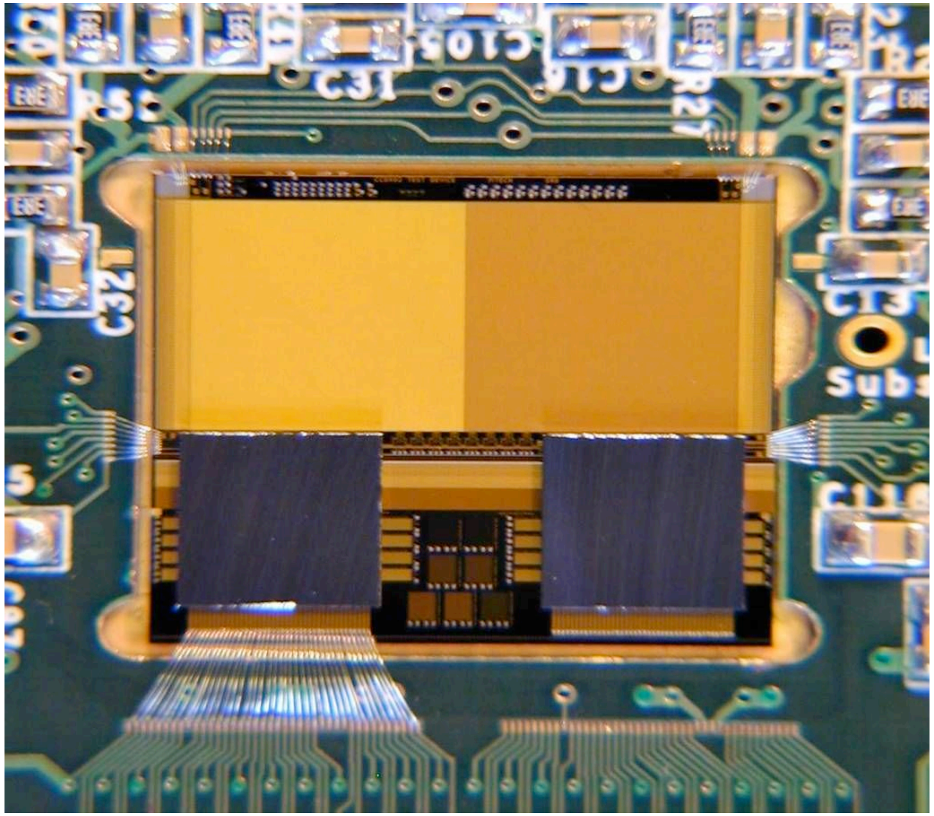
Column Parallel CCD
Readout time = (N+1)/F_{out}



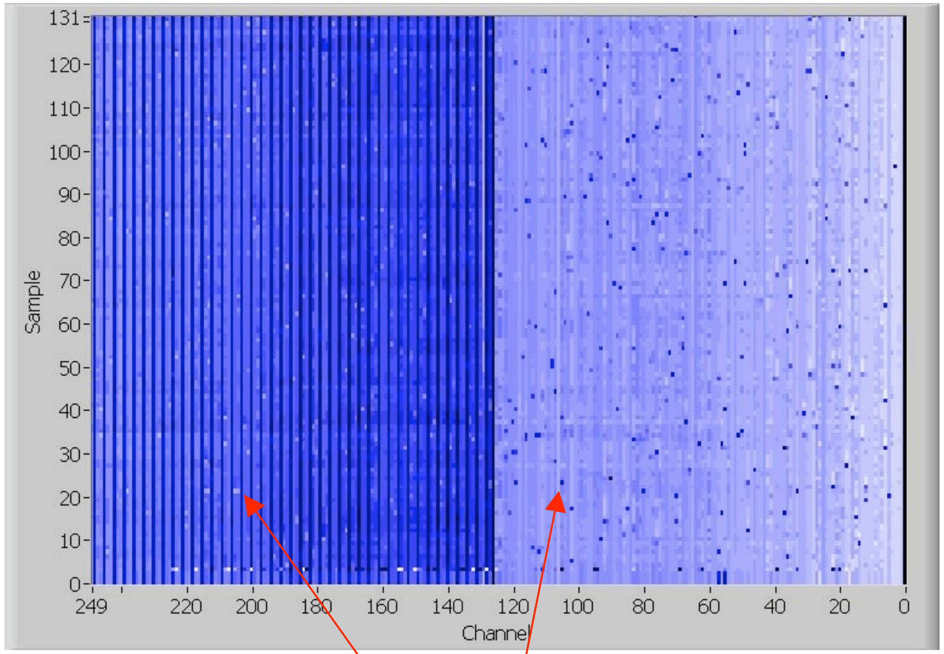
- Clock drive is real challenge

Prototype CPCCD

Chips bumped to CCD



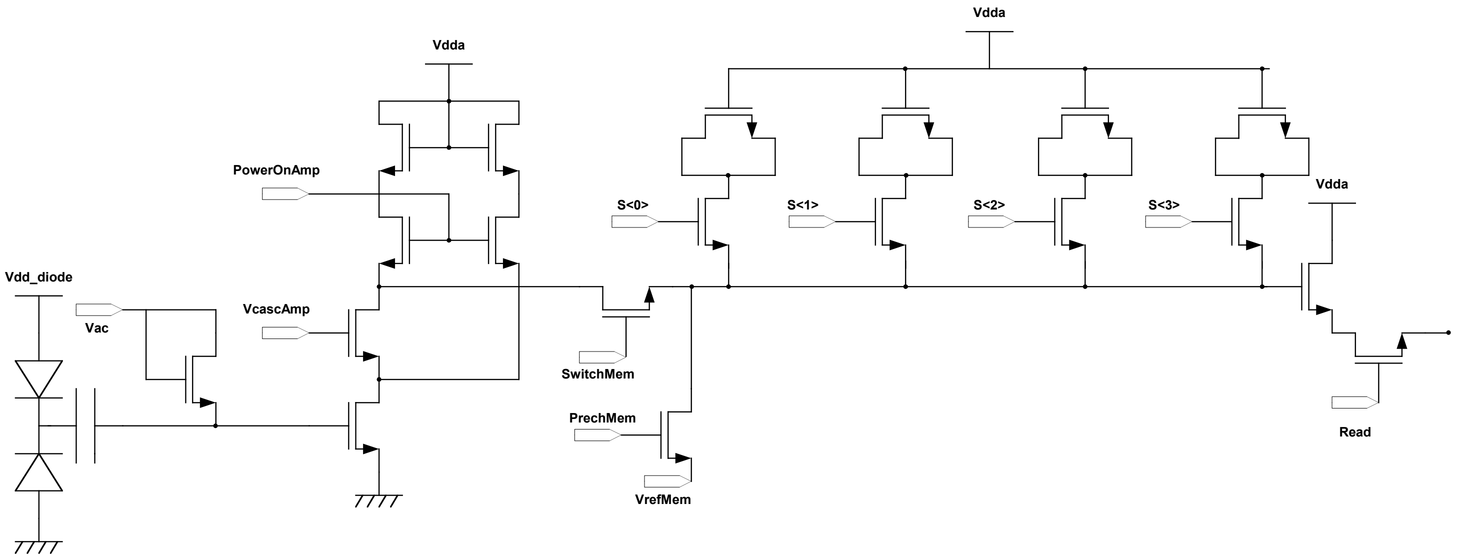
One time slice



6 keV X-rays

Next generation: faster CCDs, chips with cluster finding

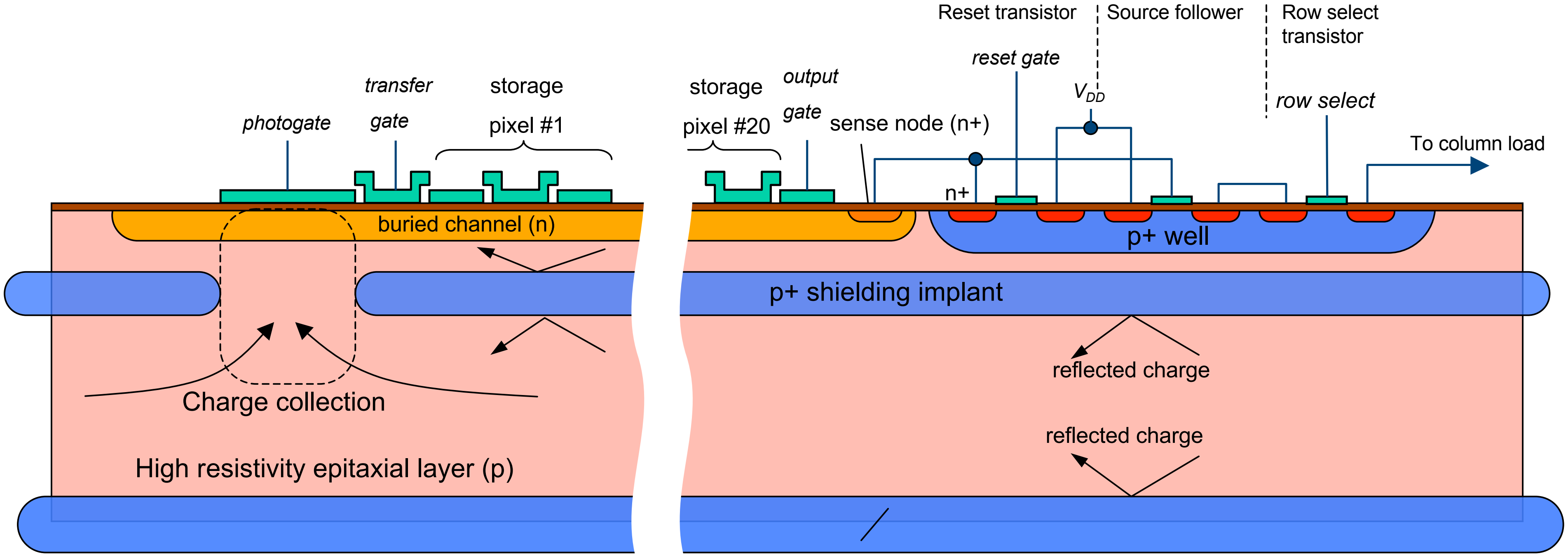
Sampling CMOS



Small CMOS feature size ⇒ more functionality within pixel

- **Multiple samples during bunch train**
- **Stored on separate capacitors**
- **Read out during quiet time**
    - ***Still susceptible to possible RF pickup***

ISIS



- **Orders of magnitude increased resistance to RF**
- **Much reduced clocking requirements**
- **Combination of CCD and CMOS technology on small pitch**

Ideal burst imager - is it practical for the ILC?

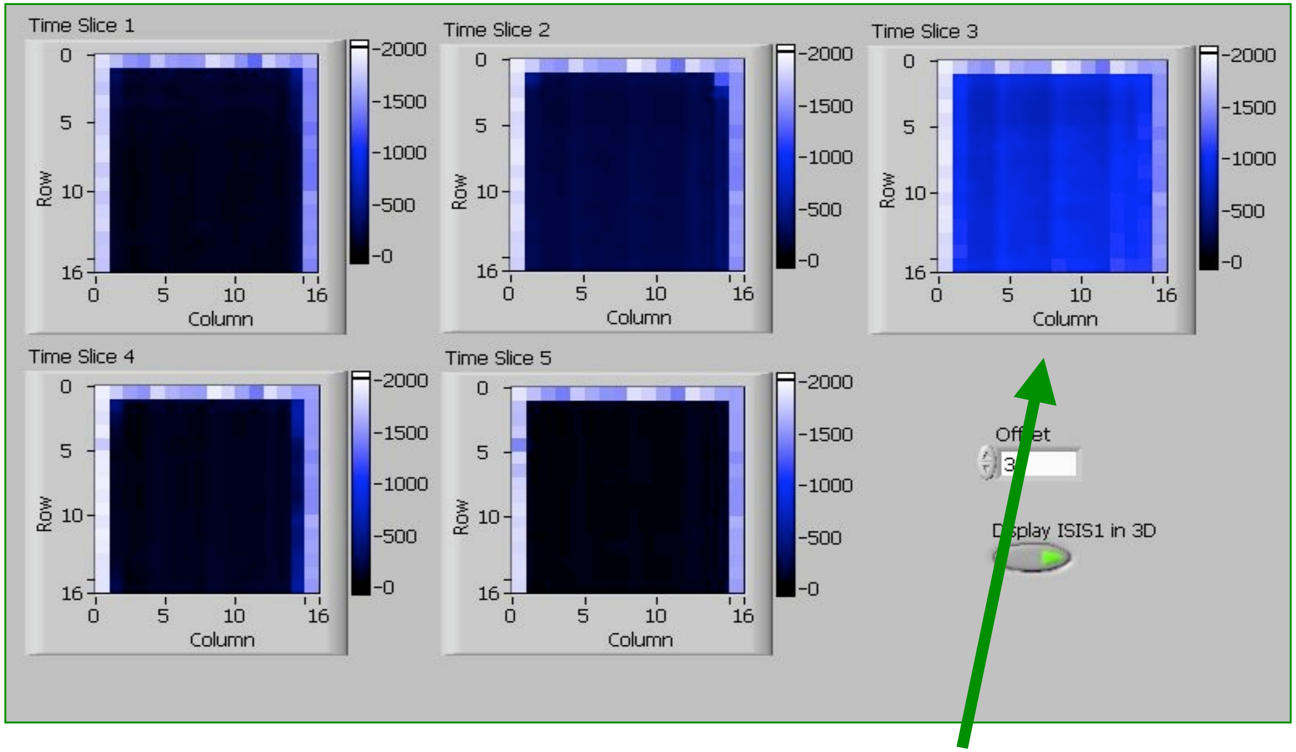
ISIS-1

Photogate 8×8μm²

5 cell CCD Register

Output and reset transistors

- **Proof-of-principle**
  - 16×16 array
  - CCD design rules



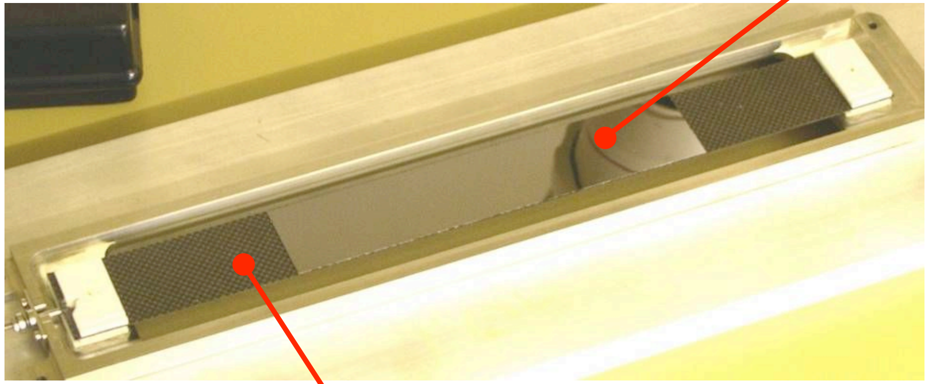
LED flash in 3rd cell

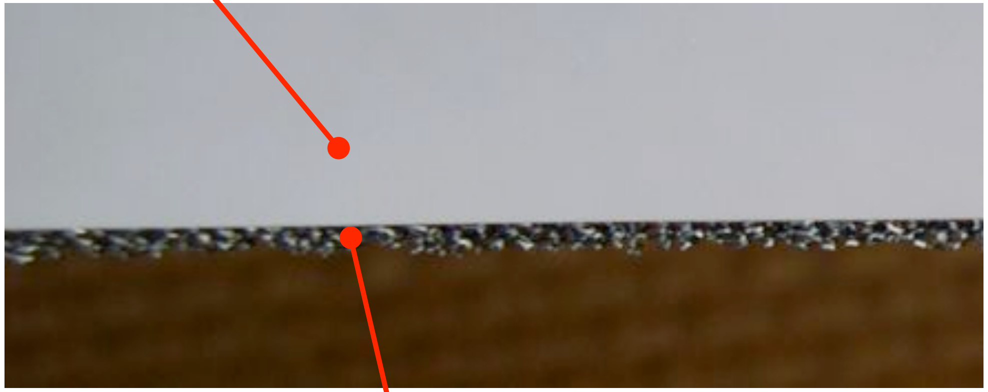
Detector Mechanics

0.1% X_0 ⇔100 μm silicon per layer!

- *Thin sensor to active layer*

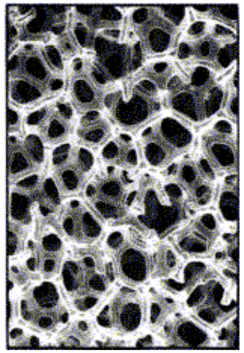
20 μm silicon





100 μm tensioned carbon fibre

1.5 mm silicon carbide foam



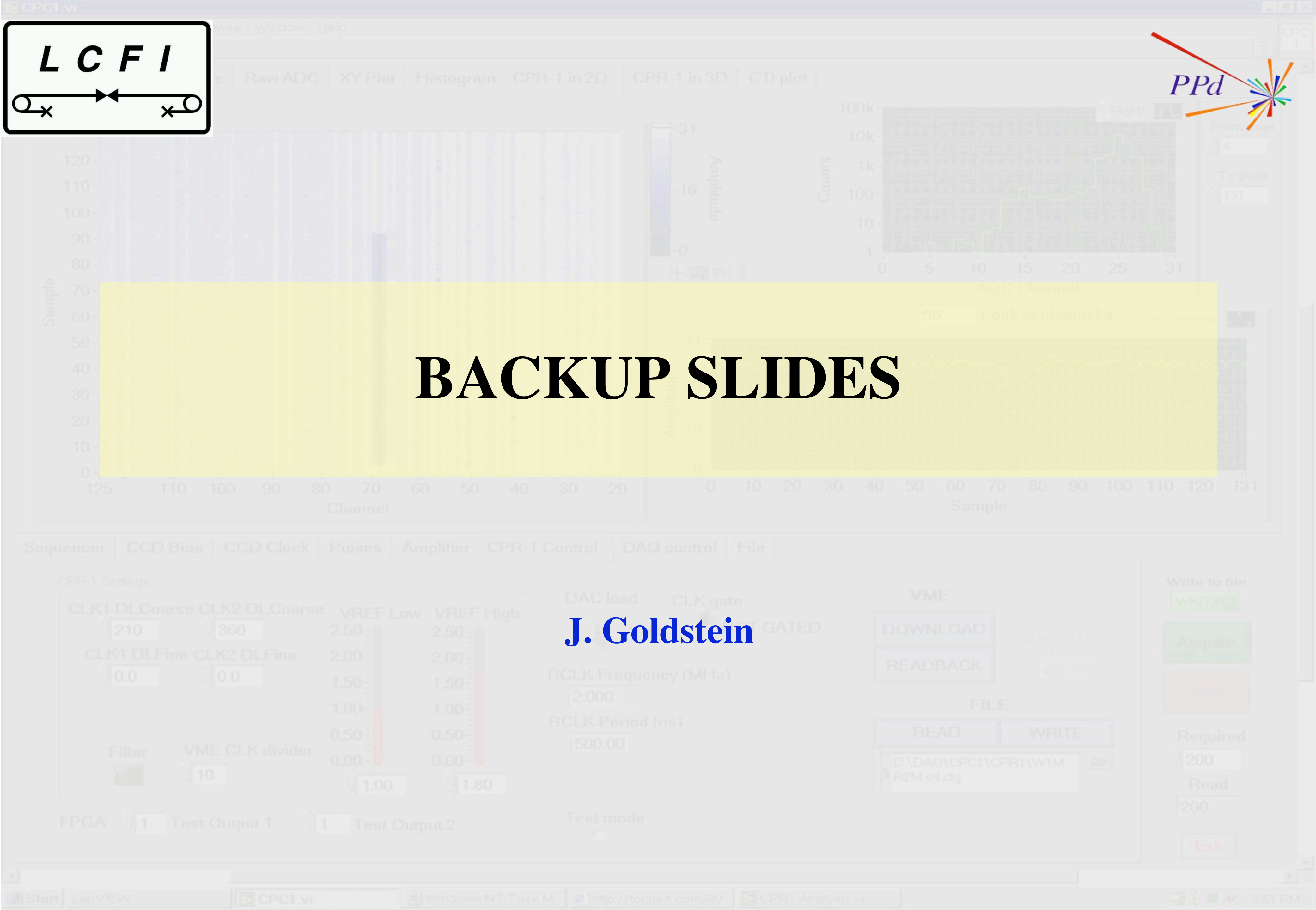
Summary

- Silicon pads for granular calorimeters
  - Active pixel sensors possible
- Silicon strips for precision tracking
  - May be only tracker
- Silicon pixels for outstanding vertexing
  - Several technology possibilities

Summary

- Silicon pads for granular calorimeters
  - Active pixel sensors possible
- Silicon strips for precision tracking
  - May be only tracker
- Silicon pixels for outstanding vertexing
  - Several technology possibilities

Next: silicon muon detectors…?



BACKUP SLIDES

J. Goldstein

LCFI Mechanical Studies

1. Thin Ladder Mechanics

- Materials and designs for ΔT ≈ 100K
- Preference for uniform material in tracking volume
- *CCDs routinely thinned to epitaxial layer*

2. Global Design

- Ensure ladder designs practical

3. Cooling

- Gas cooling has always been assumed…

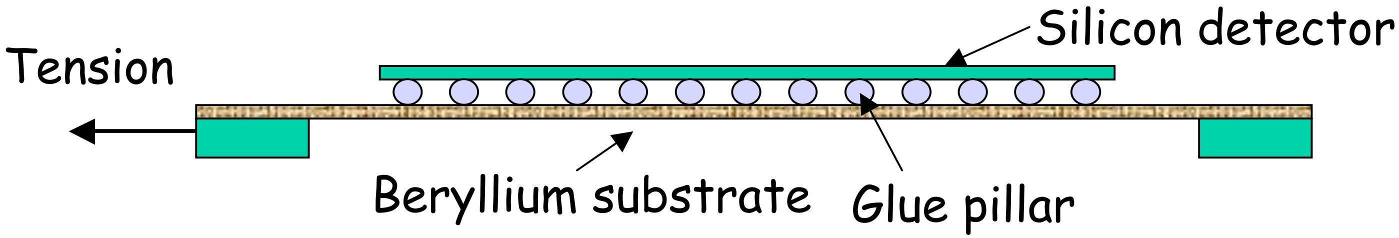
Mechanical Options

Target of 0.1% X_0 per layer

(100µm silicon equivalent)

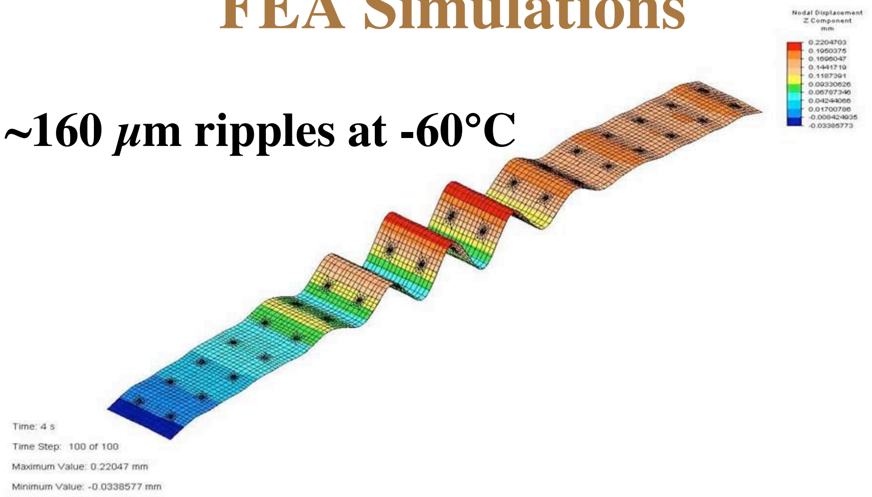
1. **Unsupported Silicon**
    - Longitudinal tensioning provides stiffness
    - No lateral stability
    - Not believed to be promising
2. **Thin Substrates**
    - Detector thinned to epitaxial layer (20µm)
    - Silicon glued to low mass substrate for lateral stability
    - Longitudinal stiffness still from tension
    - Beryllium has best specific stiffness
3. **Rigid Structures**

Mechanical Studies of Be-Si

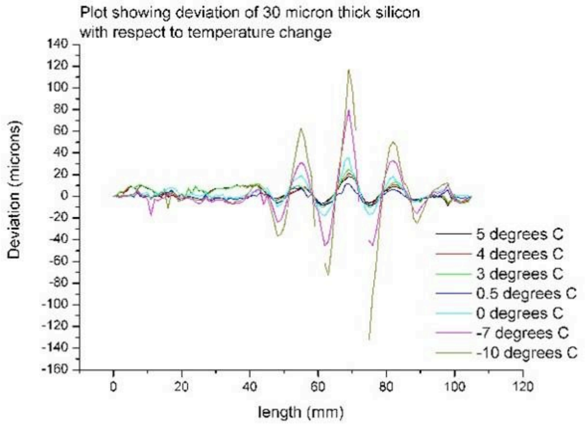


FEA Simulations

~160 μm ripples at -60°C



Physical Prototyping

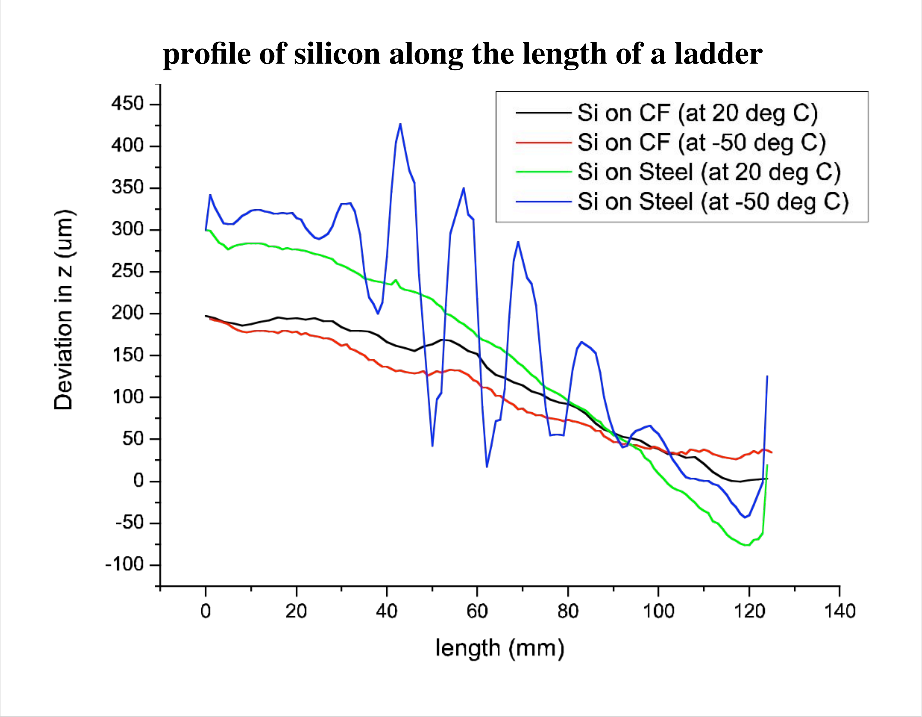


- **Good qualitative agreement**
- **Minimum thickness ~ 0.15% X_0**

Carbon Fibre Substrates

- Carbon fibre has better CTE match than beryllium

- Prototype ~ 0.09% X_0
  - – No rippling down to < 200K
  - – Lateral stability insufficient



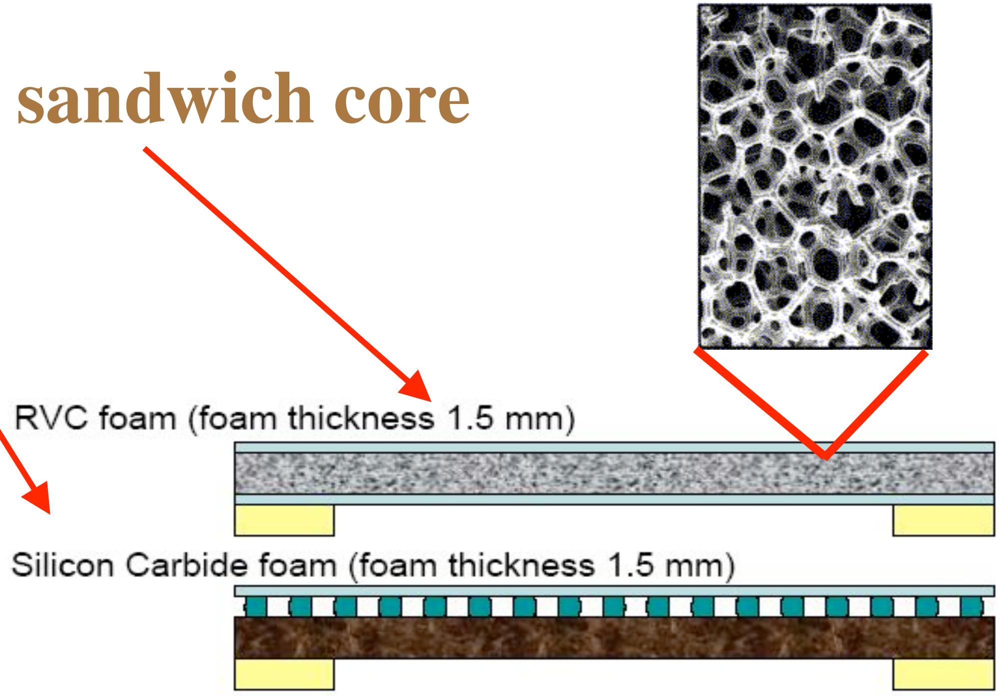
- Other thin substrates under consideration

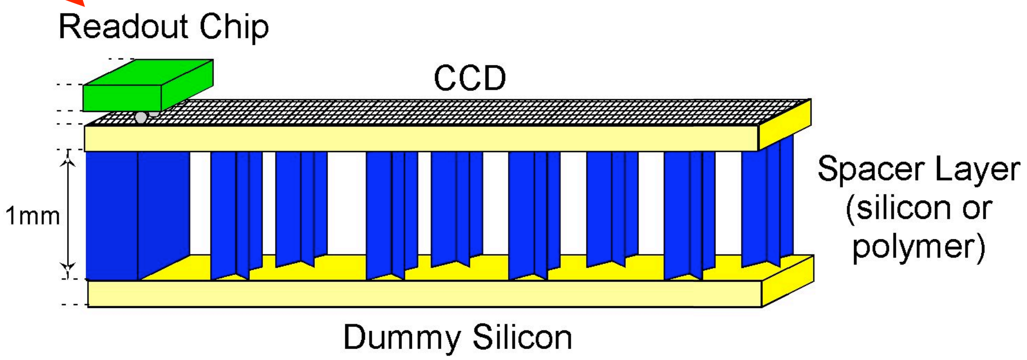
Rigid Structures

Foam: substrate or sandwich core

- **Macroscopically uniform**
- **No tensioning needed**

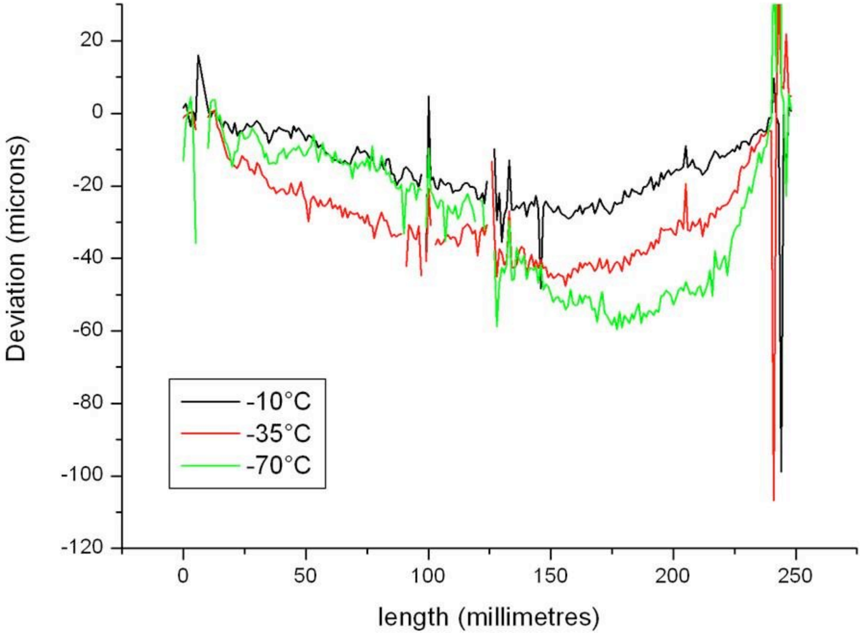
Other approaches exist

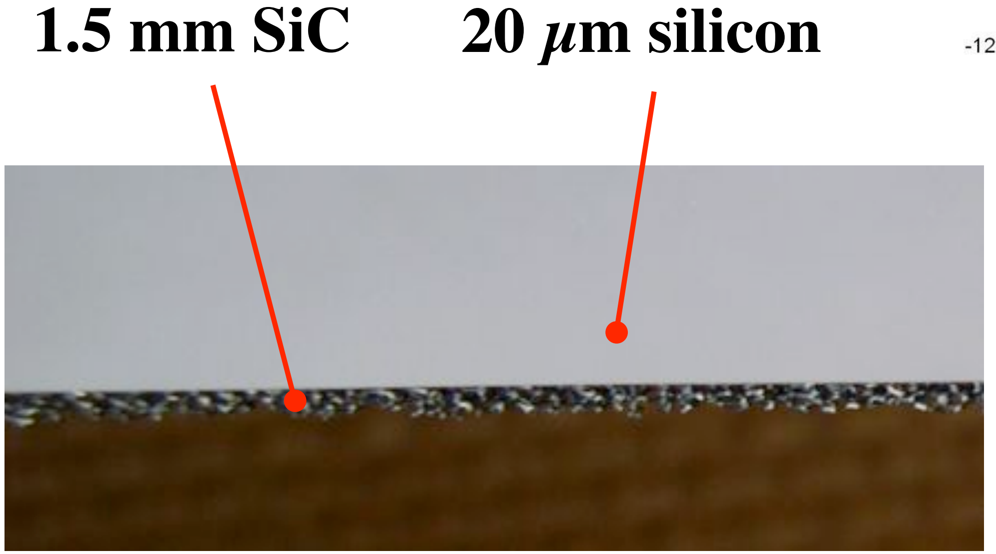




Foam Prototypes

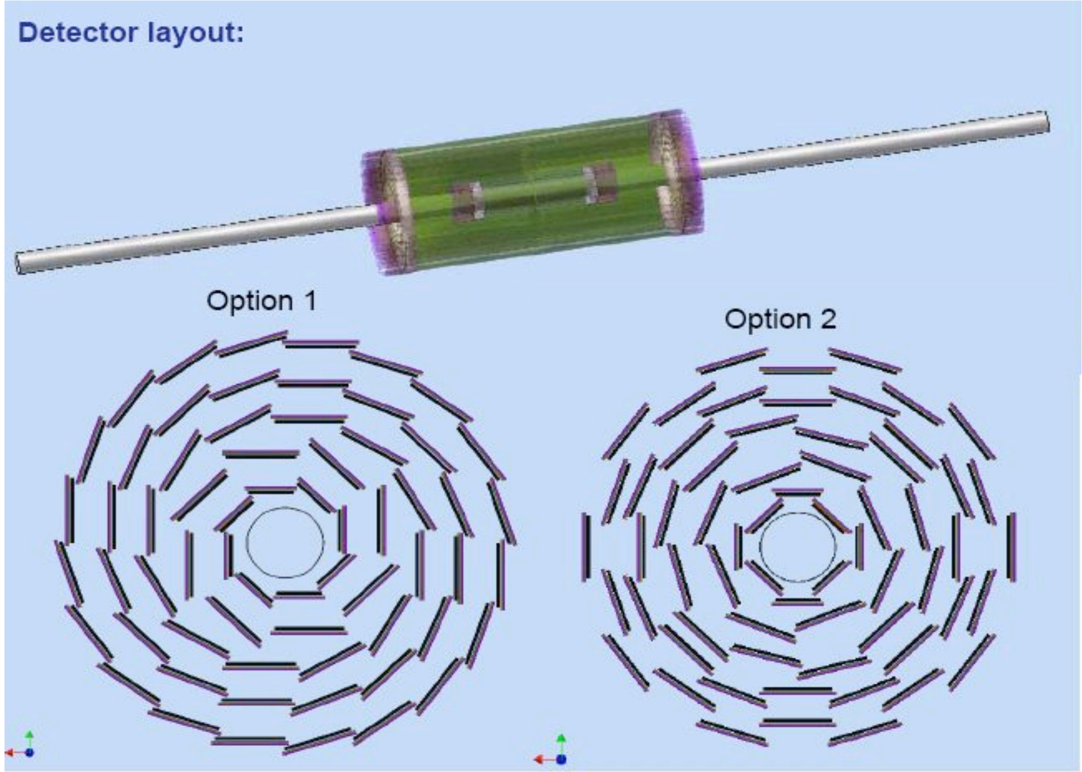
- 8% Silicon Carbide
  - Single-sided
  - 0.14% X0
  - 3-4% believed possible

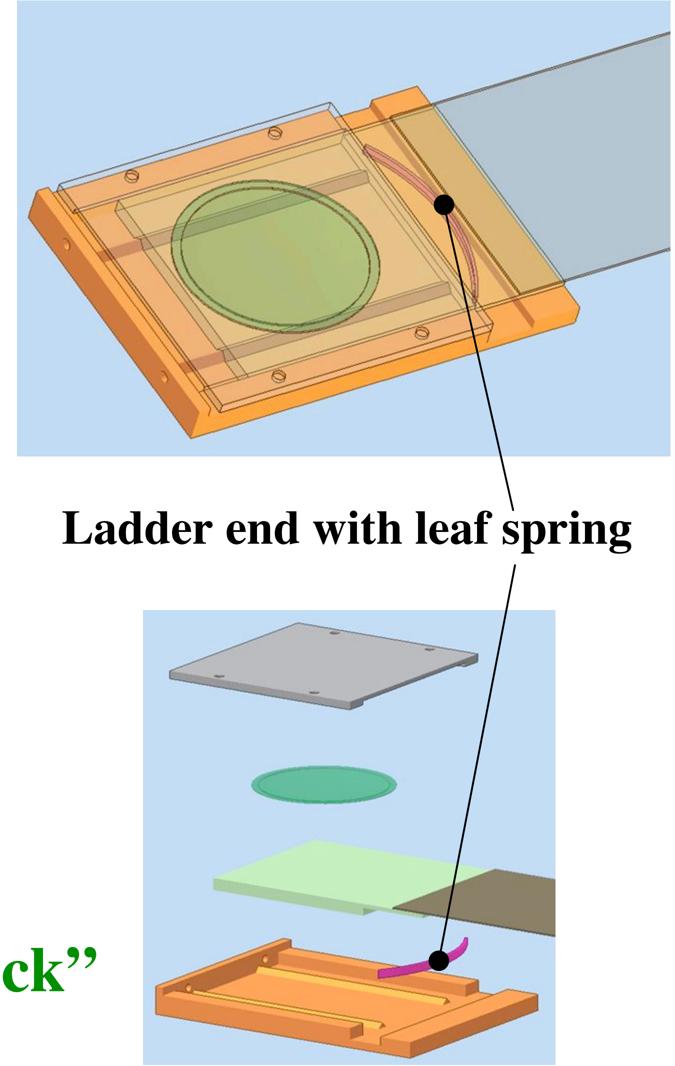




- 3% RVC
  - Sandwich
  - 0.09% X_0

Global Design Work





Ladder end with leaf spring

- **Enough detail for ladder design "sanity check"**

Sensor Research

1. Column Parallel CCDs
    - Focus so far - building on past experience
    - Readout during bunch train
    - Clock drive major challenge
2. Image Sensor with In-situ Storage
    - Increased robustness
    - Reduced driver requirements

Prototype CP CCD

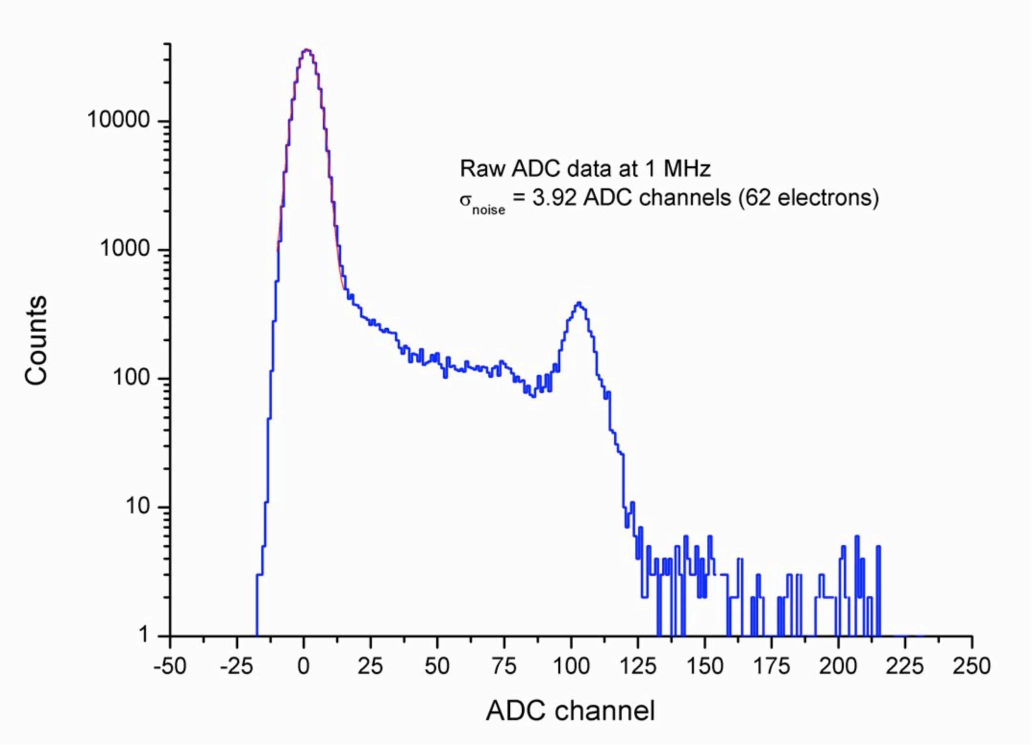
CPC-1 produced by e2v

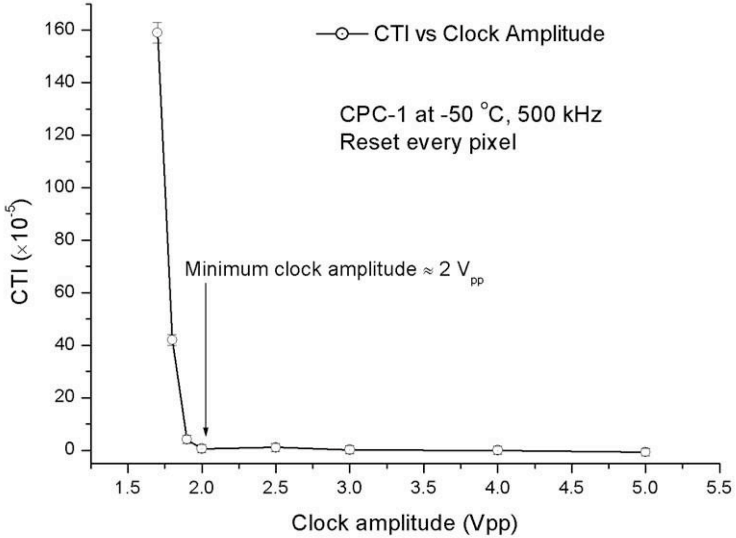
- Two phase operation
- Metal strapping for clock
- 2 different gate shapes
- 3 different types of output
- 2 different implant levels

➢*Clock with highest frequency at lowest voltage*

CPC-1 Results

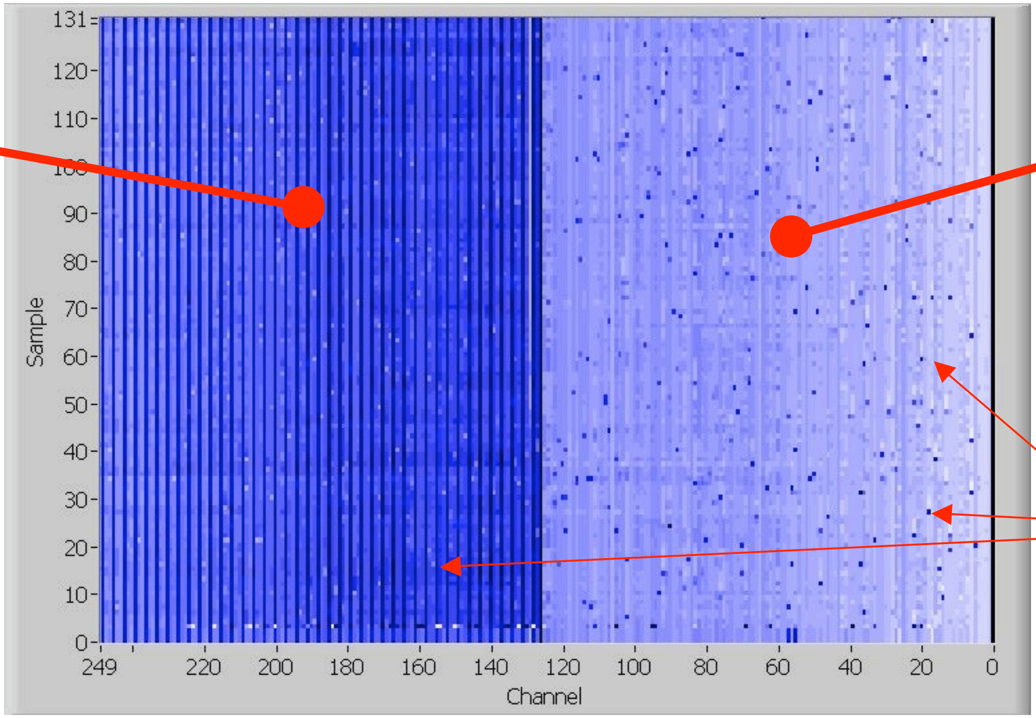
- Noise ~ 100 electrons (60 after filter)
- Minimum clock ~1.9 V





- Maximum frequency > 25 MHz
  - inherent clock asymmetry

Testing Results



Charge Amplifiers
(inverting)

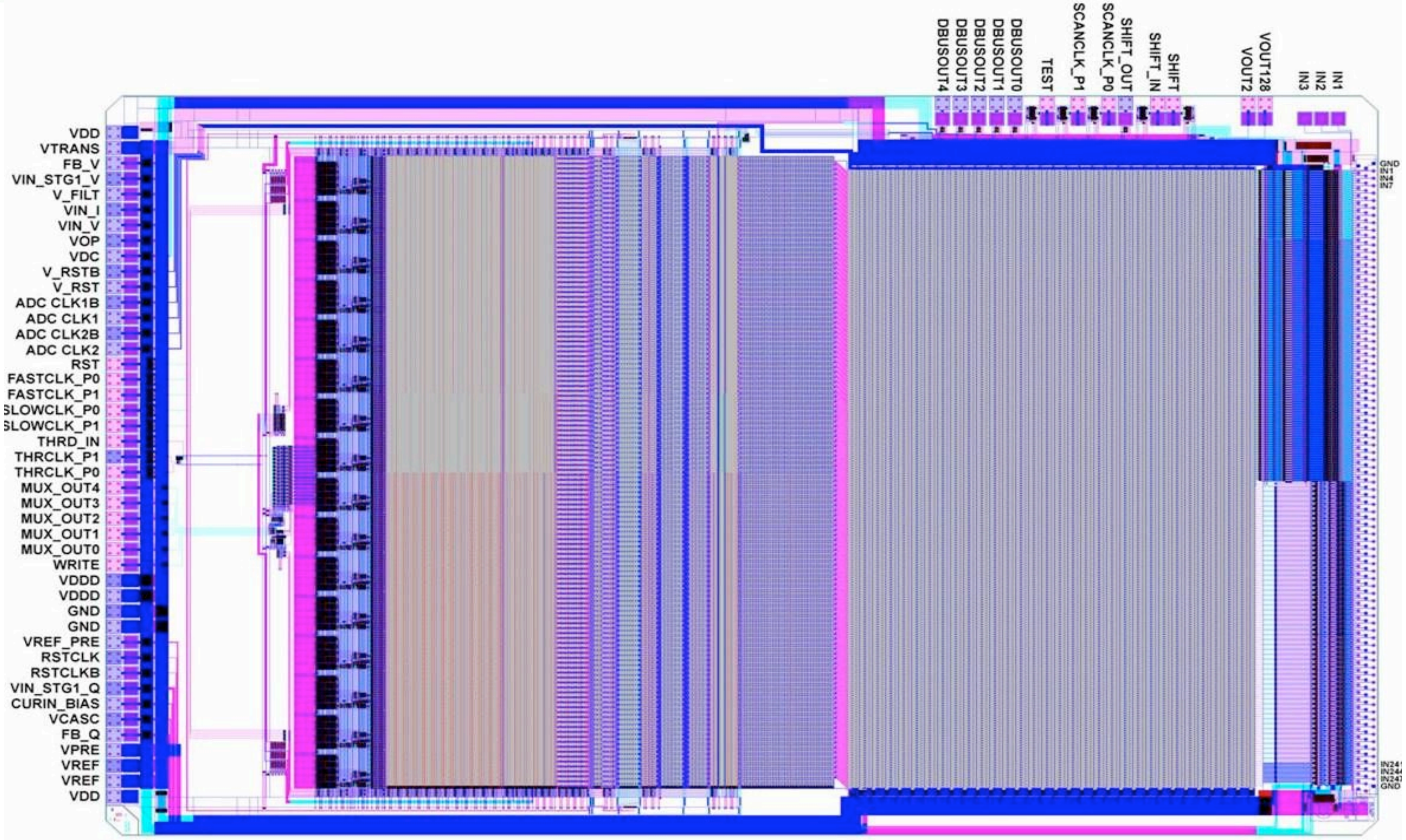
Voltage Amplifiers
(non-inverting)

6 keV X-rays

- **Charge amplifiers work**
- **Negligible noise from CPR**
- ***Column parallel operation demonstrated***

- **No signal in ~20% of voltage channels**
- **Readout chip very sensitive to timing and bias issues**
- **Gain decrease towards centre of chip**

New Readout Chip



Output

Sparsification & Multiplexing

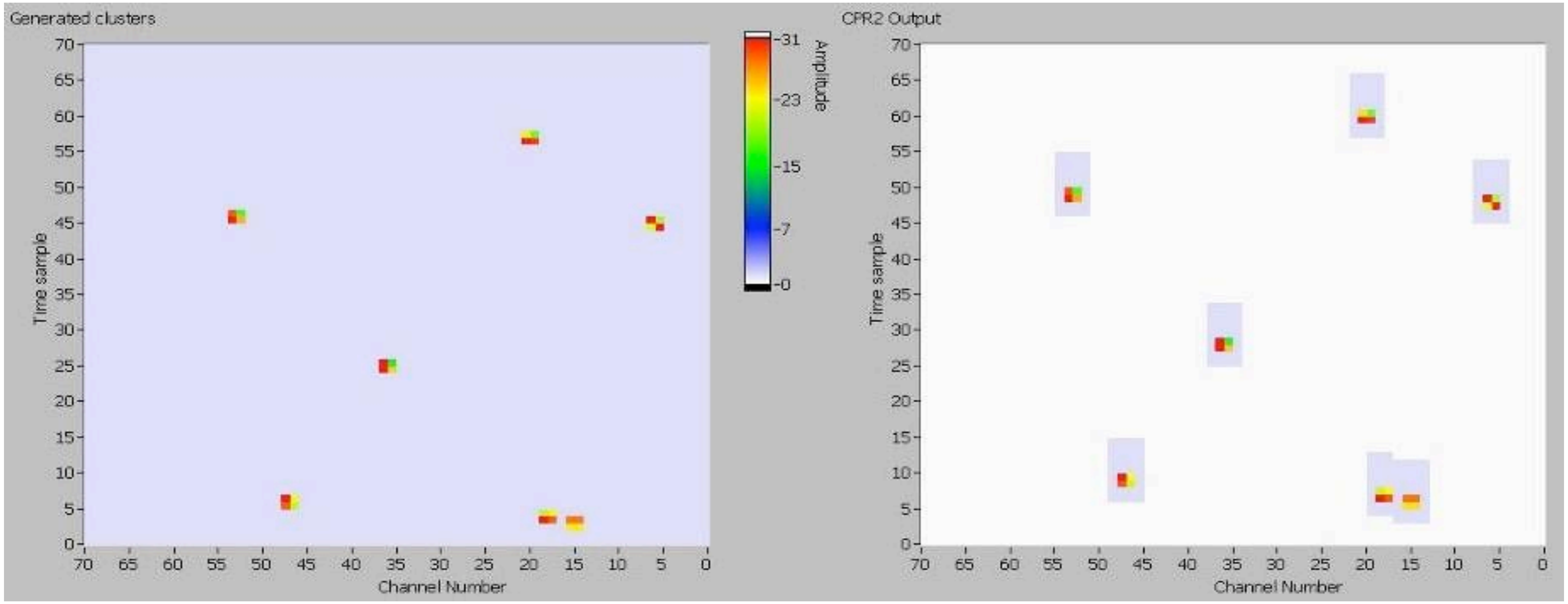
Cluster Finding

Binary Conversion

5-bit ADC

Preamp Input

CPR-2 Testing



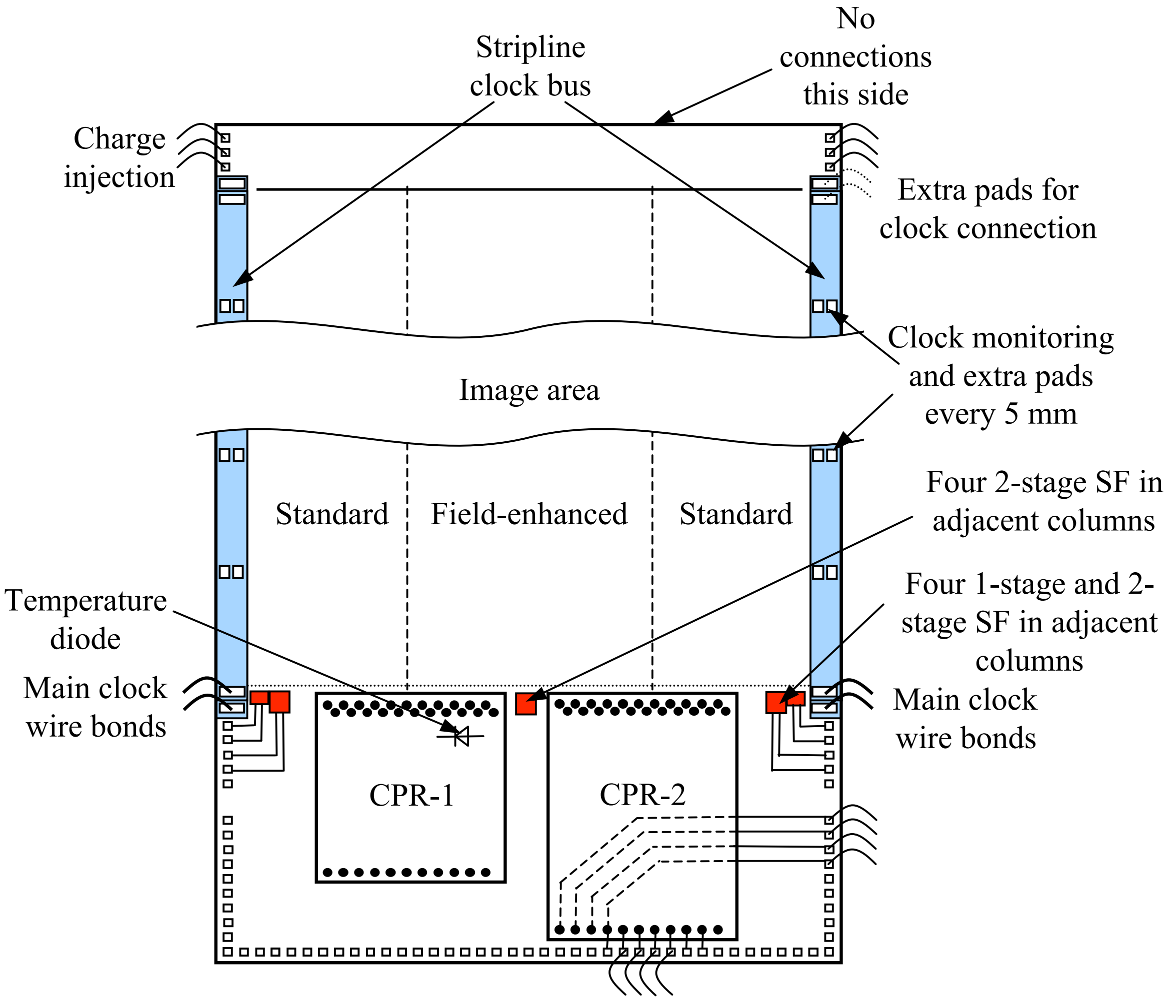
- Cluster finding logic and sparse readout
- Improved amplifiers and ADCs
- Increased robustness

The Second Generation

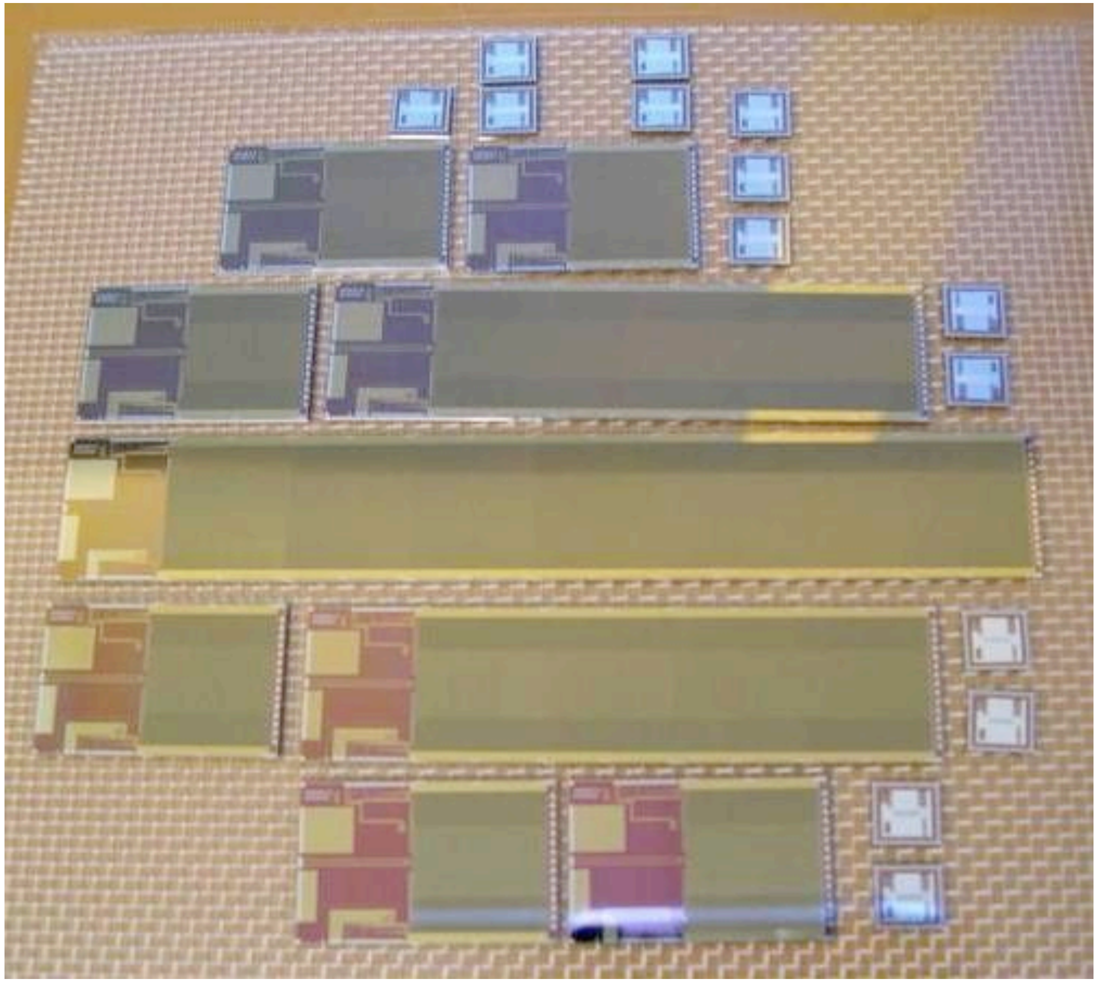
- CCDs
  - Larger and faster prototypes
  - Clock drivers
  - Radiation effects
- ASICs
  - More robust
  - Cluster finding logic
- Hostile RF environment:
  - Large EM leakage from ILC bunch train
  - Charge-voltage conversion dangerous
  - *Store multiple charge samples locally*
  - *Readout all samples during 200ms dead time*

New CPC

- **Double metal now available from e2v**
- **Symmetric clock design**
- **“Busline-free” option**
  - **Distributed clock planes**
  - **Faster**
  - **More uniform**
- **Compatible with old and new readout chips**



CPC-2 Production



- **Dedicated batch at e2v**
- **3 sizes of CPCCD**
  - ***up to 92 mm active length***
- **First devices delivered**
- **Wafers include 16×16 ISIS**