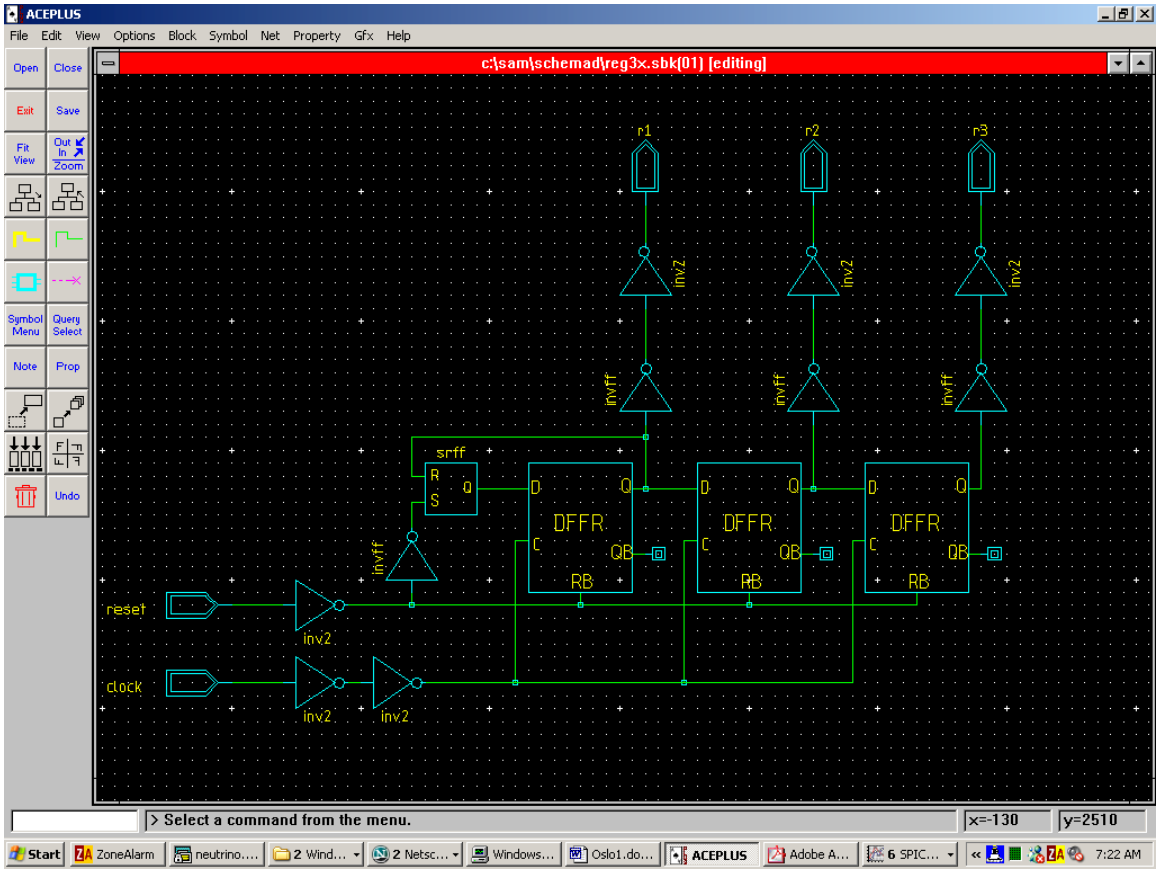
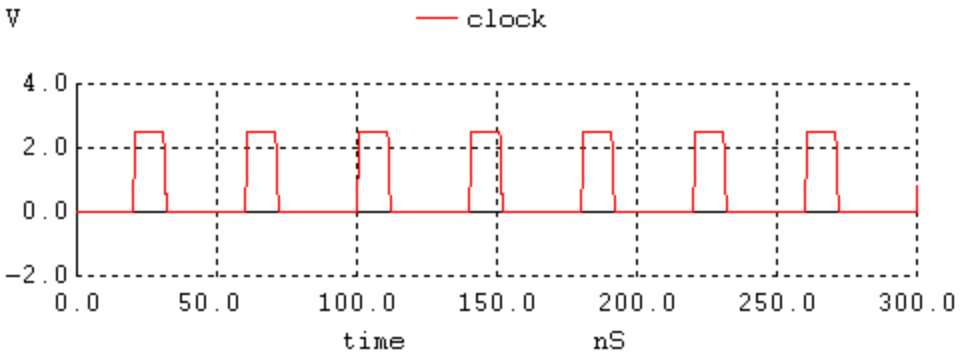
OSLO !

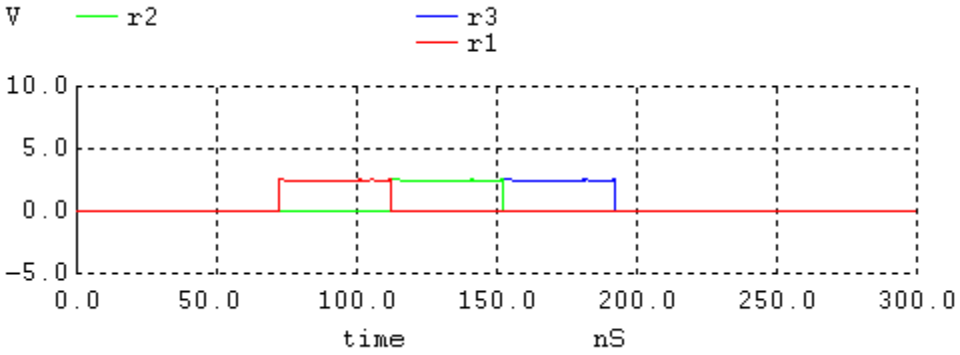
Orientation with Win-Spice 1.4.0 to simulate a 4 bit ripple counter for use in the x ray event counter. Once the schematic has been created one needs to generate a netlist using "netgen.bat" which must point the the saved schematic file (must edit two lines in the bat file). The input file must be edited to specify the stimuli (input signal), filename.txt in the WinSpice\input folder. Exicute the netgen bat file to generate a netlist, check to see how it looks. Edit the simulate.txt file to point at the 4 required files to carry out the Spice application. Use the "plot x y z etc " command in the spice command line file to view the resulting signals.

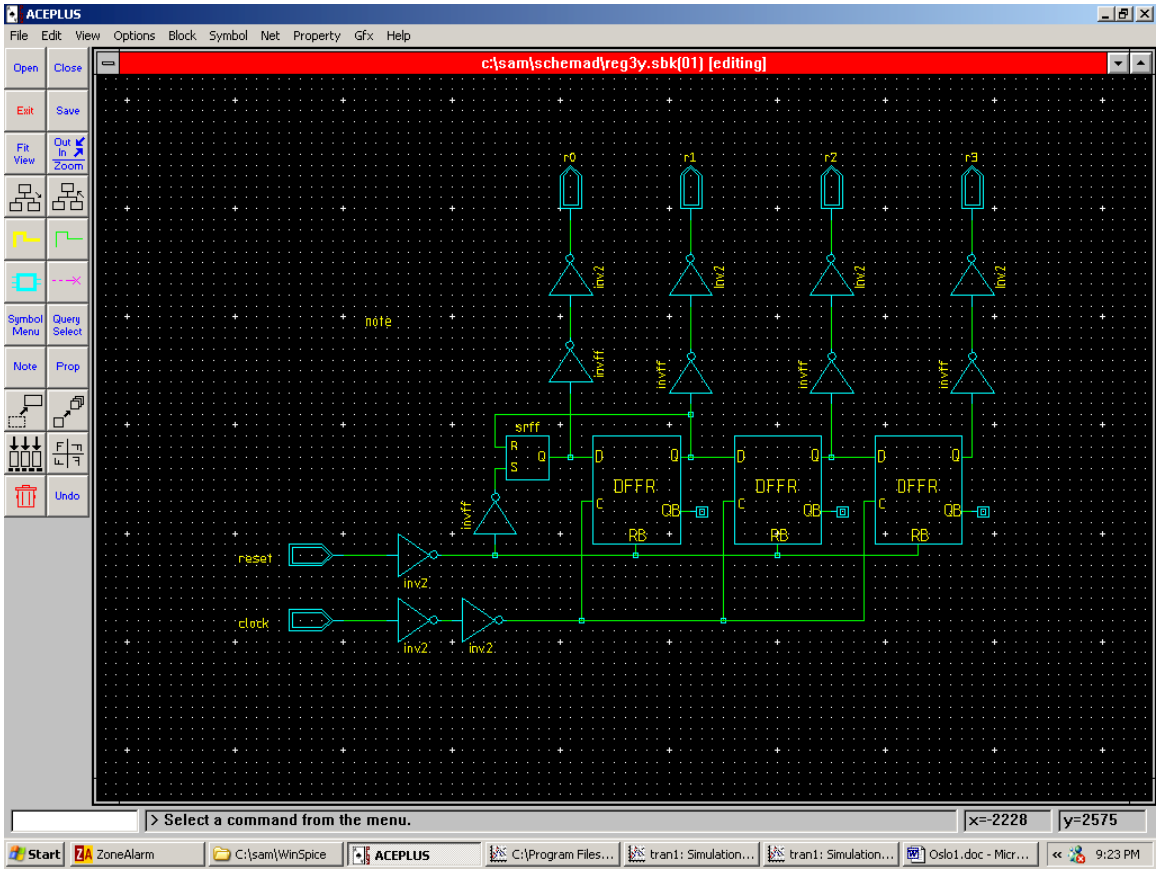
The digital readout of 18 bit ripple counters from a 4x4 pixel array will use a row/columb selector with a multiplexer/shift register. Pixel register 01 will be latched into an 18 bit shift register and shifted followed by pixel 02 finishing up with pixel 16. The shift rate must be 130 Mhz.

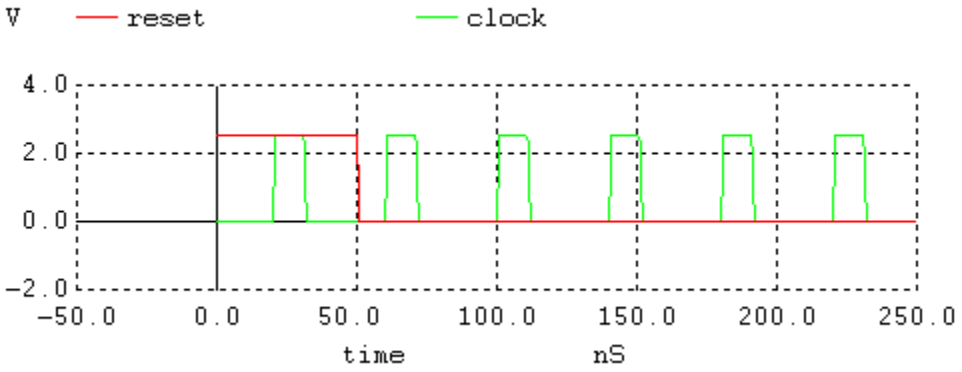
A 3 stage shift register with a bit seed will be used to address the separate pixels.

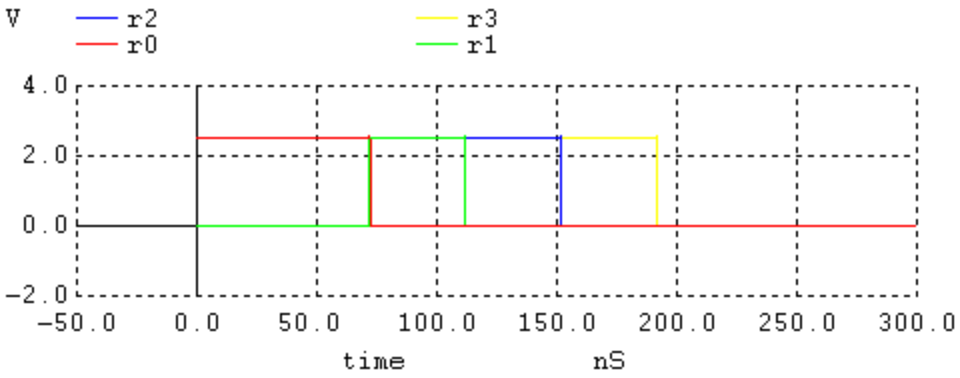


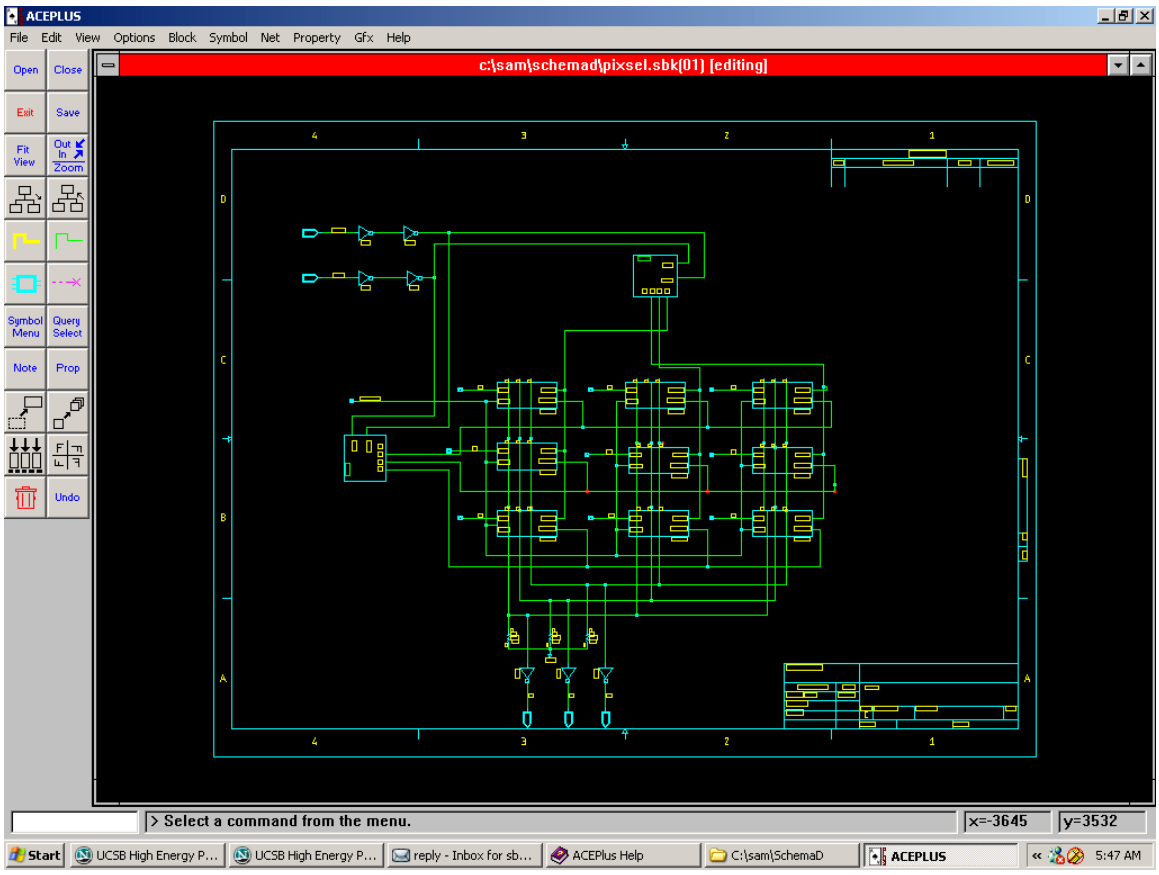

V
clock
4.0
2.0
0.0
-2.0
0.0
50.0
100.0
150.0
200.0
250.0
300.0
time
nS


V
r2
r3
r1
10.0
5.0
0.0
-5.0
0.0
50.0
100.0
150.0
200.0
250.0
300.0
time
nS


ACEPLUS
File Edit View Options Block Symbol Net Property Gfx Help
c:\sam\schemad\reg3y.sbk(01) [editing]
Open
Close
Exit
Save
Fit View
Out In Zoom
Symbol Menu
Query Select
Note
Prop
Undo
r0
r1
r2
r3
inv2
nvff
srff
DFFR
reset
clock
note
> Select a command from the menu.
x=-2228
y=2575
Start
ZoneAlarm
C:\sam\WinSpice
ACEPLUS
C:\Program Files...
tran1: Simulation...
tran1: Simulation...
Oslo1.doc - Micr...
9:23 PM

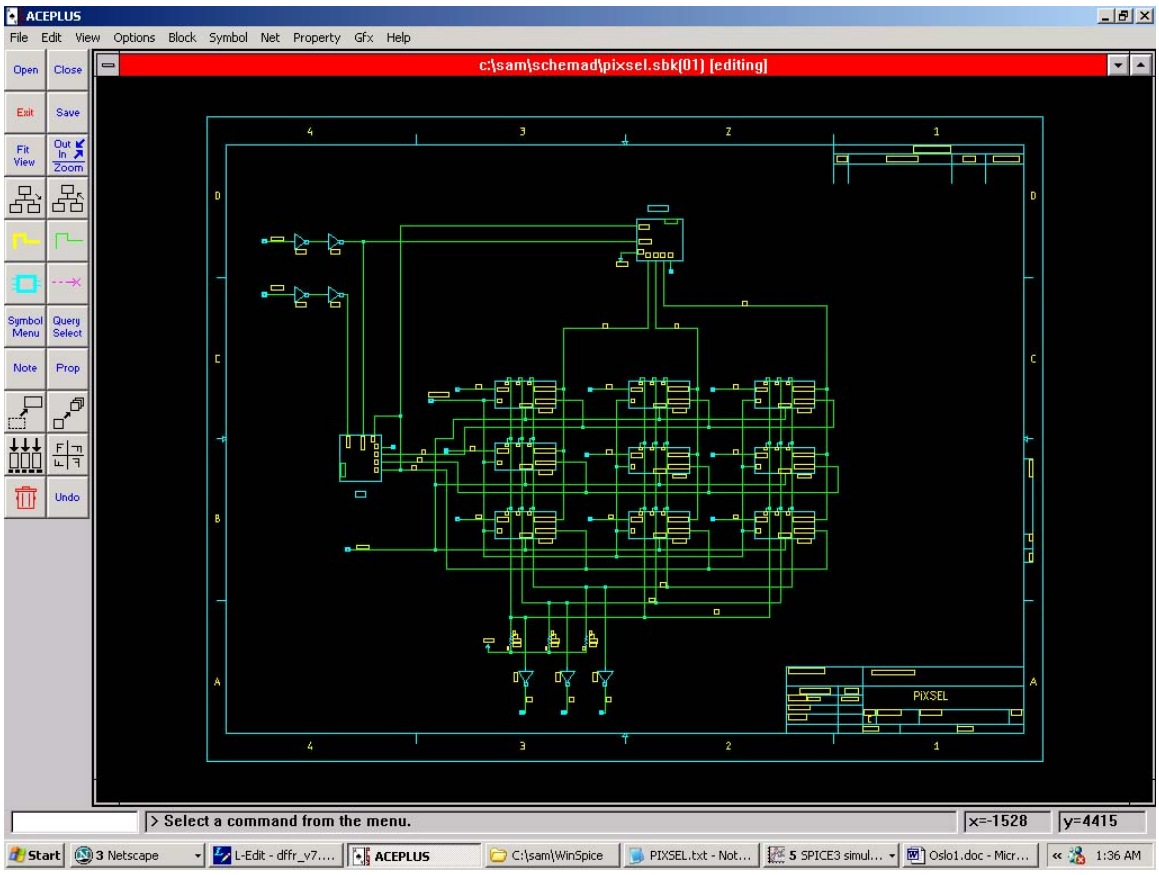

V
reset
clock
4.0
2.0
0.0
-2.0
-50.0
0.0
50.0
100.0
150.0
200.0
250.0
time
nS

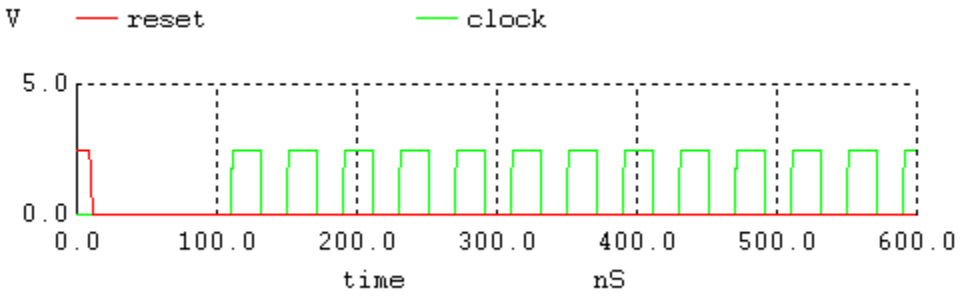




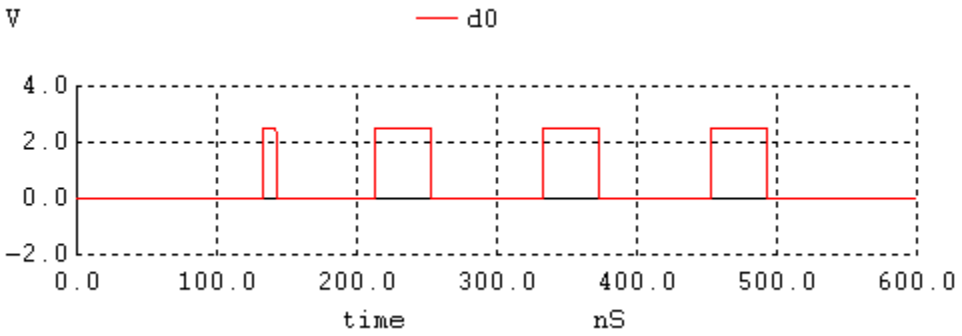
A Feedback FB input was added to 3bit columb and row shift registers and r3 from row register is used as the clock for the columb register, r3 from the row register is also fed back to the

Feedback input of the same register with results shown below following simulation.

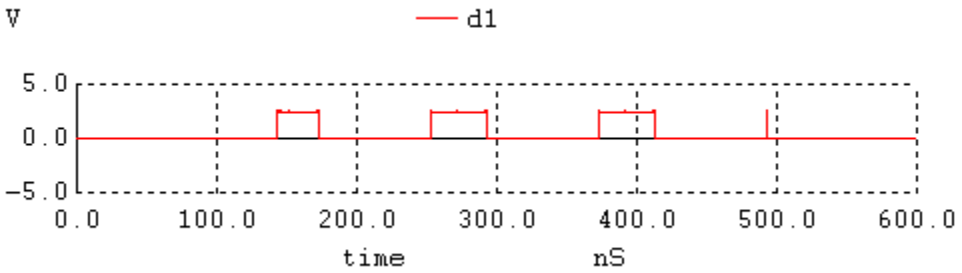




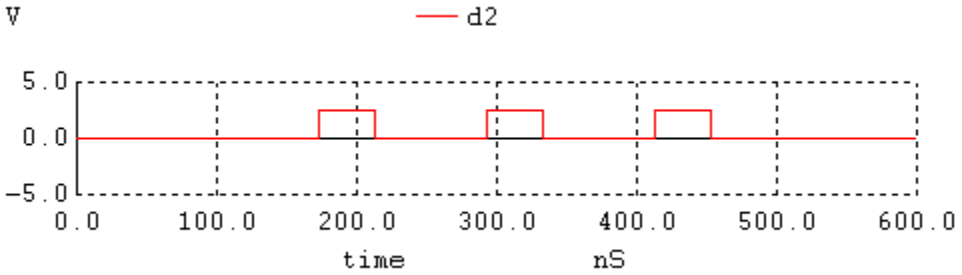
Reset and clear are the same above.



We have a glitch at 140 ns on d0.



We have a small glitch at 490ns on the d1 line.



The Pixel readout is shown below decoded;

2	2	2
4	4	4
1	1	1

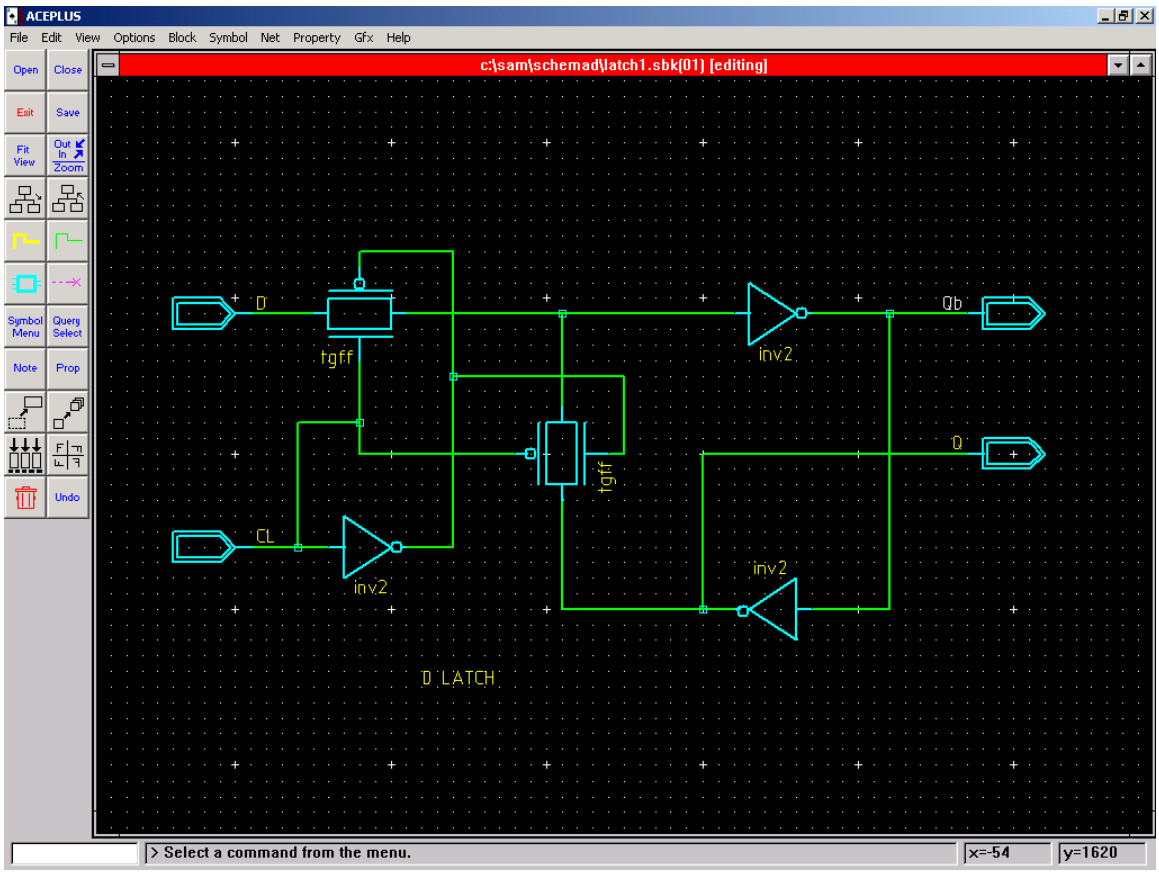
The Test Inputs used in the Spice simulation for the 3x3 pixel array decoder was generated with the test file below;

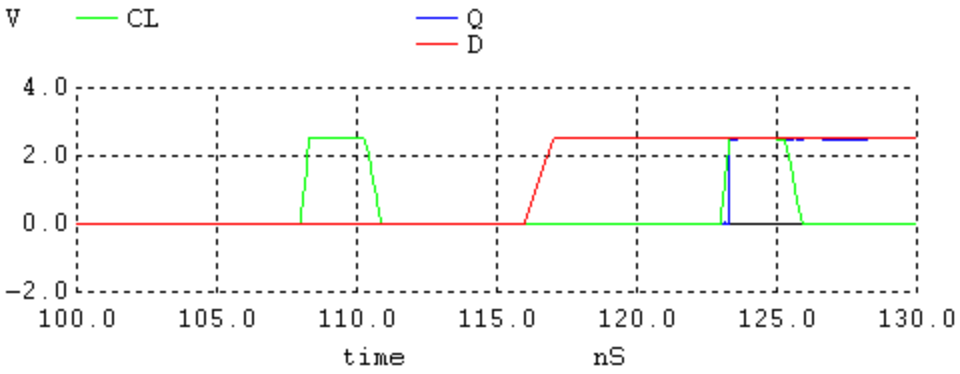
****** test1 input deck *********

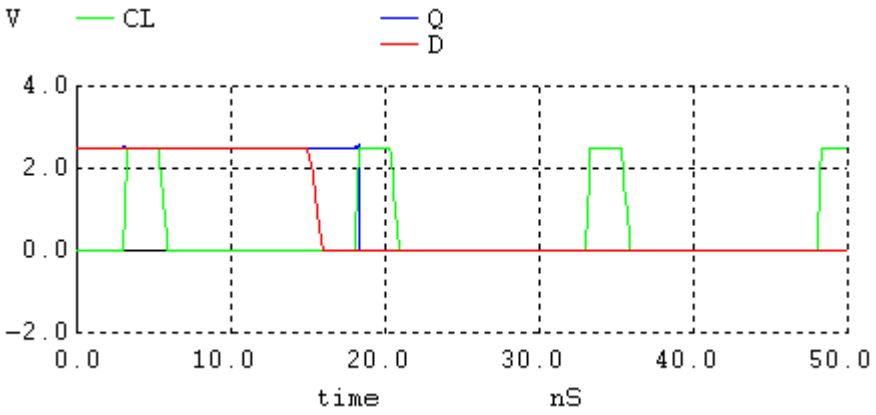
```
vreset reset 0 pulse 2.5 0 10n 1n 1n 1 2
vclock clock 0 pulse 0 2.5 110n 1n 1n 20n 40ns
vclear clear 0 pulse 2.5 0  10n 1n 1n 1 2
vcount_en count_en 0 pulse 0 2.5 25n 1n 1n
80ns 1
vp0 p0 0 pulse 0 2.5 30n 1n 1n 10n 20n
vp1 p1 0 pulse 0 2.5 30n 1n 1n 5n 10n
vp2 p2 0 pulse 0 2.5 30n 1n 1n 15n 30n
vp3 p3 0 pulse 0 2.5 30n 1n 1n 10n 20n
vp4 p4 0 pulse 0 2.5 30n 1n 1n 5n 10n
vp5 p5 0 pulse 0 2.5 30n 1n 1n 15n 30n
vp6 p6 0 pulse 0 2.5 30n 1n 1n 10n 20n
vp7 p7 0 pulse 0 2.5 30n 1n 1n 5n 10n
vp8 p8 0 pulse 0 2.5 30n 1n 1n 15n 30n

.control
```

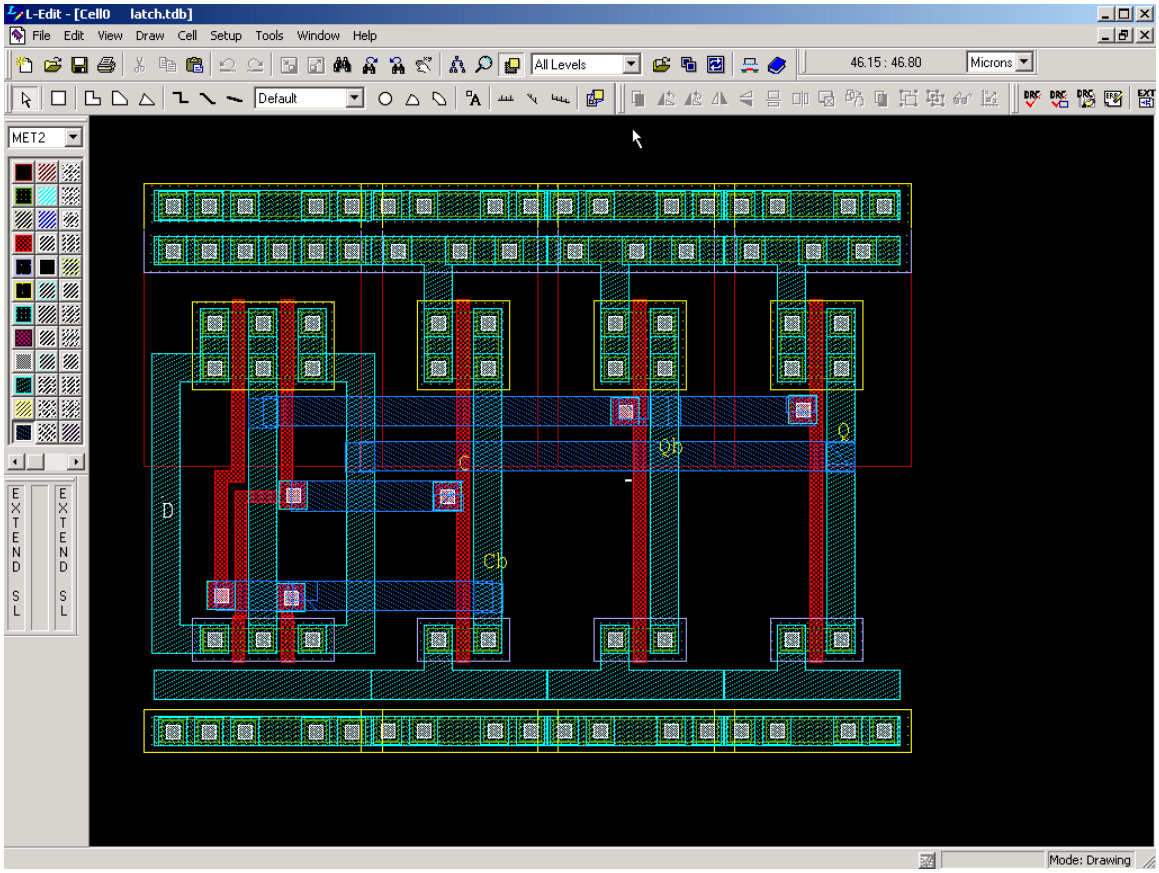
tran 1ns 600n

.endc

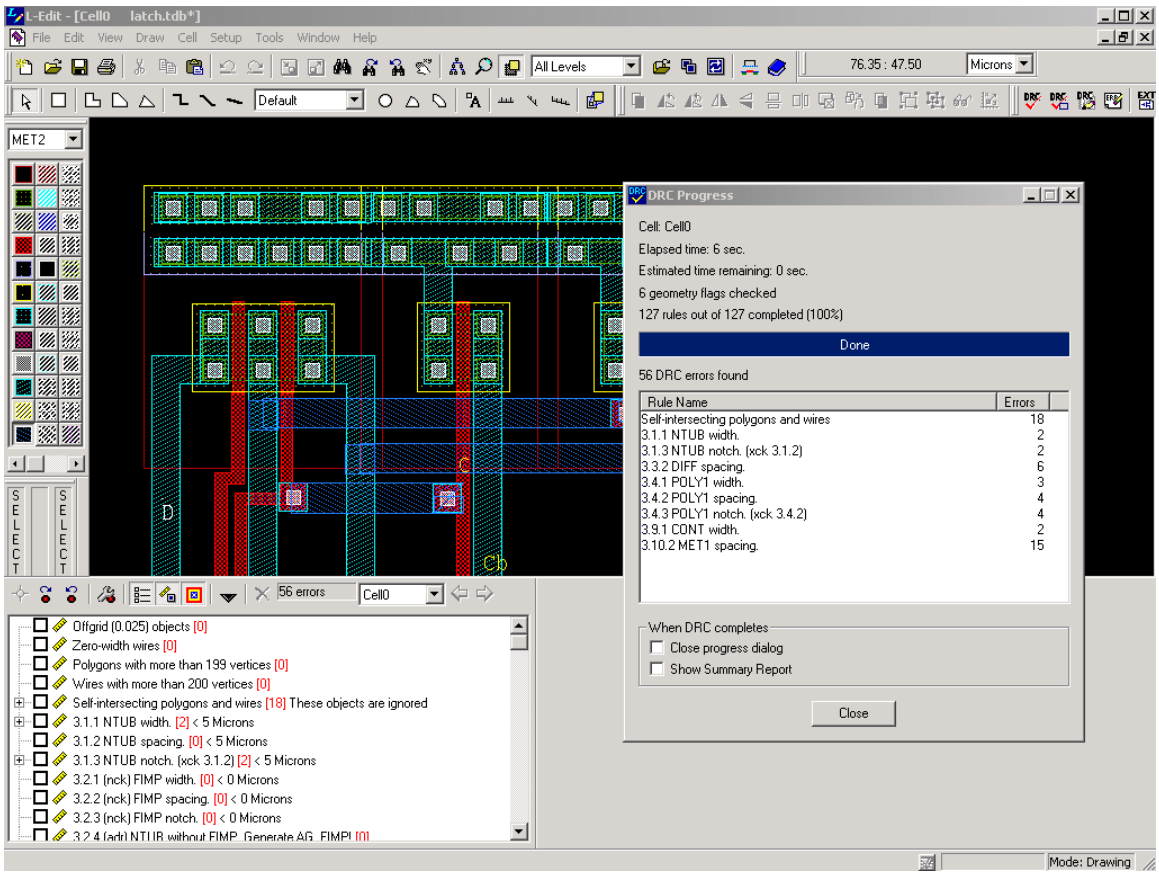



V
CL
Q
D
4.0
2.0
0.0
-2.0
100.0
105.0
110.0
115.0
120.0
125.0
130.0
time
nS


V
CL
Q
D
4.0
2.0
0.0
-2.0
0.0
10.0
20.0
30.0
40.0
50.0
time
nS



This is the layout on Si using the Oester Microsystems process. From left to right we have a SPDT transmission gate followed by three inverters with appropriate interconnects.



The Latch has 56 DRC errors so no simulation can proceed until they are taken care of.