DFFR Simulation Results

- Ts: Setup Time > 0.4ns
- Th: Hold Time > 0.1ns
- Tclk-min: Minimum clock pulse width > 0.35ns
- Fclk-max: Max Clock Freq < 980 Mhz
- Td: Delay Time <0.5ns
- Tc: Clear Time >0.4ns
- Size [4*4.5+4*4.5+2*6]*12=48*12=576um^2

  - Note: 10 ps rise times on test clock