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The BaBar silicon vertex tracker☆

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Abstract

The Silicon Vertex Tracker (SVT) for the BaBar experiment at the PEP-II asymmetric B factory is a 5-layer device based on double-sided, AC-coupled silicon strip detectors. It is read out by a custom IC, the AToM chip, that can simultaneously acquire, digitize and transmit data. The main purpose of the SVT is to accurately measure the decay position of the B mesons that are produced, which is essential for extracting CP asymmetries. Here, we report on the SVT design as well as progress on its fabrication and assembly.

Keywords: SVT; BaBar experiment; Silicon strip detectors

1. Introduction

1.1. PEP-II and the BaBar experiment

The main physics objectives of the BaBar experiment [1] in the PEP-II e^+e^- colliding beam storage ring [2] at SLAC are to study CP violation in B decays and to over-constrain the CKM quark mixing matrix of the standard model. The $B\bar{B}$ pairs from $\Upsilon(4S)$ decay are produced coherently, so the difference (Δt) between the decay times of the B and the $\bar{B}$ must be measured for each event in order to measure CP violating asymmetries. The PEP-II beam energies are unequal, thus the B mesons are boosted along the higher energy e^- beam direction and travel a measurable distance. The BaBar experiment will measure the decay point of each of the B mesons using the Silicon Vertex Tracker (SVT).

1.2. SVT design constraints and requirements

1.2.1. PEP-II

The PEP-II beam energies are 3.109 and 9.000 GeV for the e^+ and e^- beams, respectively, which corresponds to $\beta\gamma = 0.56$ for the $\Upsilon(4S)$ in the lab. The PEP-II design luminosity is 3×10^{33} cm^{-2} s^{-1} with a peak luminosity of 10^{34} cm^{-2} s^{-1}. Such high luminosities are achieved by separating the beams into a large number of bunches, where the bunches have a spacing of 1.26 m or a crossing period of 4.2 ns.

The relatively short bunch spacing places several constraints on the SVT design. First, in order to collide the beams head-on (0° crossing angle) at the interaction point and only at the interaction point, permanent dipole (B1) magnets must be placed $\pm$ 20 cm from the interaction point. The presence of the B1 magnets limits the fiducial region of the SVT to $17.2^\circ < \theta < 150^\circ$ where $\theta = 0$ is the forward, high-energy beam direction. The B1 magnets will be installed before the SVT, so the SVT must be clam-shelled into place. Secondly, the short crossing period means there are effectively continuous interactions. The SVT front-end electronics must be able to simultaneously acquire, digitize, and read-out in order to maintain high efficiency.

The main PEP-II background in the region occupied by the SVT is from lost beam particles which produce electromagnetic showers in the detector material. At the radius of the first layer of silicon, the expected average dose is 33 krad/yr with a peak value of 240 krad/yr at $\phi = 0$. This means the front-end read-out IC must be radiation hard. The SVT must be able to withstand at least 10 times the expected annual radiation dose.

1.2.2. BaBar *physics*

The most important SVT resolution requirement comes from the need to measure the decay position of both B mesons along the beam direction in order to determine the time difference Δt between the two B decays. Monte Carlo studies have shown that the precision of a CP asymmetry measurement is degraded by only 10% if the resolution on Δz, the difference in the B decay points along the beam direction, is about $\frac{1}{2}$ the average separation between the decay points, which is 250 μm at PEP-II [3]. This corresponds to a single vertex resolution of 80 μm or better.

For tracking in BaBar, the momentum range of interest is $p < 5$ GeV/c and $p_T < 2.6$ GeV/c. The acceptance must be as low in momentum as possible, since B daughters can have $p < 100$ MeV/c

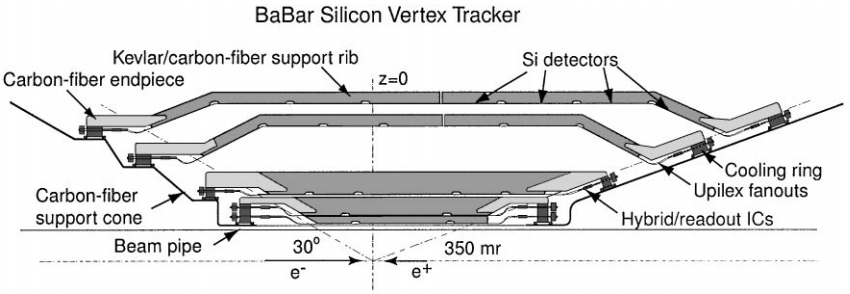

Fig. 1. A cross-section view of the upper half of the SVT.

(e.g. the π from $B \to D^*X$ followed by $D^* \to D\pi$). At such low momenta, multiple Coulomb scattering can seriously affect tracking performance, therefore the amount of inactive material in the fiducial region must be kept to a minimum. Particles with $p_T < 100$ MeV/c cannot be reconstructed in the BaBar drift chamber, so the SVT must be capable of stand-alone tracking for very low momentum particles.

2. SVT description

The SVT has been described in several recent publications [4–6]. We review the basic design in this section. The SVT design consists of 5 layers of double-sided, AC-coupled, 300 μm thick silicon wafers, where the stereo angle is 90°. The strips are read out by a custom IC (the AToM chip) which is able to simultaneously acquire, digitize, and read out data. The silicon wafers are electrically connected to the AToM chips via flexible fanout circuits which are glued to the wafers and the High Density Interconnects (HDIs) or hybrids. Fig. 1 shows the top half of a cross-section view of the SVT.

The first three layers are in a barrel geometry, divided into a pinwheel of sextants. The first layer is as close as possible to the Be beam pipe in order to minimize the effects of multiple scattering in the beam pipe, which is about 1.06% X_0 for a 90° track. The primary function of the first three layers is to measure the z impact parameter of tracks, crucial for measuring Δz of the two B hadron decay vertices. They also give the most accurate measure of the track angles ϕ and θ as well as the x–y impact parameter.

The outer two layers are composed of 16 and 18 arched modules of silicon wafers. As Fig. 1 shows, the end wafers of each module are wedge shaped and angled towards the beam. The arching reduces the angle of incidence for far forward and backward tracks and maximizes the solid angle coverage, for the area of silicon used. The main functions of the outer two layers are to provide additional measurements for pattern recognition and to enable stand-alone tracking for tracks too low in momentum ($p_T < 100$ MeV/c) to be reconstructed in the drift chamber.

The HDIs for each module are mounted on brass cooling rings, which are in turn mounted on carbon-fiber support cones surrounding the B1 permanent dipole magnets. The HDIs are electrically connected to the back-end readout electronics by multi-layer flexible circuits, which are required, rather than more conventional cables, due to the extremely limited space near the B1 magnets. Rigid support for the SVT is provided by a carbon-fiber space frame.

In the following sections, we will describe components of the SVT in more detail with results on their fabrication and performance.

3. Silicon wafers

The silicon wafers for the SVT, manufactured at Micron Semiconductor,[1] are 300 μm thick with high-resistivity n bulk material. The n^+ and p^+ strip implants are AC-coupled to the front-end

[1] Micron Semiconductor Ltd., Lancing, UK.

Table 1
Silicon wafer implant type, strip pitch, and readout pitch for the five SVT layers. Layers 4 and 5 have wedge-shaped wafers at the ends of each module which gives a variable pitch in ϕ. The ϕ-side for layers 1 and 2 is split into regions with and without floating strips, as explained in the text

Layer	Side	Implant type	Strip pitch (μm)	Readout pitch (μm)
1	ϕ	n	50	50 and 100
	z	p	50	100
2	ϕ	n	55	55 and 110
	z	p	50	100
3	ϕ	n	55	110
	z	p	50	100
4	ϕ	p	50 to 41	100 to 82
	z	n	105	210
5	ϕ	p	50 to 41	100 to 82
	z	n	105	210

electronics by silicon-dioxide layers sandwiched between the strip implants and the aluminum strips on the surface of the detectors. Bias resistors for the strips are built into the wafers through polysilicon structures connecting the bias ring and the strip implants. The n^+ strips are isolated by a thin p^+ ring ("p-stop") surrounding each n^+ strip. There are six different wafer designs for the SVT; one for each of the inner three layers and three for the outer layers, including a wedge-shaped wafer for the arched region at the ends.

The strip and readout pitch for each layer are given in Table 1. The original plan was not to have floating strips on the ϕ-side for layers 1–3. Recent studies have shown that without floating strips the inner layers are susceptible to significant inefficiencies for tracks with a large incidence angle if the noise is higher than expected. On the side of the wafer where the Lorentz angle is opposite the direction of the incidence angle, the ionization charge is spread out, rather than concentrated, thus reducing the signal size per readout strip. By bonding only every other readout strip in the inefficient region, the signal size is effectively doubled due to the charge sharing from the unbonded, floating strips. With the new configuration, the inefficiency is removed. A preliminary study indicates that the change in the track impact parameter resolution due to the new configuration ranges from a 10% degradation for near normal incidence tracks to a 10% improvement for large incidence angle tracks.

We have received from Micron all 340 of the silicon wafers needed to complete the SVT plus additional spares. After receipt from Micron, each wafer is fully characterized as described in Ref. [7]. The operating voltage, total strip current, and guard-ring current must be reasonably stable and low. For each readout strip, the inter-strip and AC-decoupling capacitance as well as the leakage current and series resistance of the metal layer is measured. If a strip does not meet the specifications, it is considered inefficient. The number of inefficient strips on each side of the detector must be below 3%.

Table 2 lists the average values for the inter-strip, AC-decoupling, and implant-to-back capacitance and the series resistance of the Al strips. The bias resistors vary from wafer to wafer, but are typically between 4 and 8 MΩ. The total strip leakage current is below 100 nA/cm^2.

Test structures from early prototypes manufactured by CSEM[2] were irradiated with a 1 MRad dose of photons to test the durability of the detectors [8]. The inter-strip capacitance increase after irradiation was no greater than 17% and the backside capacitance was stable. The current density increased by no more than 350 nA/cm^2, most of which was due to thermally generated surface currents.

4. Detector fanout assemblies

After the silicon wafers are individually tested and graded, they are glued to the flexible fanouts. We refer to these units as Detector Fanout Assemblies (DFAs). Each SVT module has a forward and a backward-facing DFA. Each DFA has between 2 and 4 silicon wafers.

[2] Centre Suisse d'Electronique et de Microtechnologie SA, Neuchâtel, Switzerland.

Table 2
Average measured properties for the SVT wafers

Implant type	Strip pitch (μm)	Inter-strip capacitance (pF/cm)	AC decoupling capacitance (pF/cm)	Implant-to-back capacitance (pF/cm)	Series resistance of metal (Ω)
n	50	1.0	20		
n	55	1.0	22	0.19	12.5
n	105	1.0	34	0.36	6.25
p	50	1.1	43	0.17	7.3

The flexible fanout circuits [9] electrically connect the silicon strips to the front-end electronics (the AToM chips). The z-side fanouts also realize the $\times 2$ ganging in layers 4 and 5. The fanouts substrates are 50 μm thick and made of Upilex,[3] which is a Kapton-like material. The conductive traces consist of a 4.5 μm Cu on top of a 150 nm Cr adhesion layer. The Cu layer is covered with another 150 nm Cr adhesion layer followed by less than 1 μm of Au. The z-side fanout covers nearly the entire surface of the wafers, however the material of the fanout contributes less than 0.03% of a radiation length on average. The capacitance of the fanout traces is 0.52 pF/cm which is about $\frac{1}{2}$ the inter-strip capacitance in the silicon wafers.

After the fanouts are glued to the silicon wafers, the strips are wire-bonded to the fanout traces and the ϕ-side strips are wire-bonded across the gaps between wafers. After bonding, the DFAs are tested for faults, such as pinholes and p-stop shorts, which are described below.

All 104 of the DFAs required to build the SVT are complete with spares, which is over 0.3 million wire-bonds. The DFAs have been tested for faults after assembly. Below, we describe some of the types of faults and the fraction of channels which they affect.

A break in the AC coupling capacitor, which causes a short between the aluminum strip and the strip implant, is referred to as a "pinhole". Pinholes can be from manufacturing defects or from bonding with too much power. About 1–2% of the channels were found to have pinholes, most of which existed before bonding. Strips with pinholes are disconnected from the readout electronics.

A short between the aluminum strip and the p-stop for n-side strips is referred to as a "p-stop short". P-stop shorts can be from manufacturing defects, but more often they are caused when the bond-foot on the silicon is offset on the pad towards a p-stop and the bond is done with too much power, thus breaking through the oxide layer. About 0.5% of the channels for the inner 3 layers had p-stop shorts. The amount of p-stop shorts in the outer two layers was negligible due to the larger strip pitch.

Other types of faults include high current strips, damaged or obscured bond pads, breaks in the fanout traces, and poor inter-strip insulation for n-strips. The fraction of channels per DFA with any kind of fault is about 2–4%.

5. High density interconnects

The High-Density Interconnects (HDIs), or hybrids, hold the front-end readout electronics (AToM chips) of the SVT [10]. The HDIs are responsible for cooling the AToM chips and serve as the mechanical interface for the modules. The HDIs reside in the region between the support cones and the active region of the SVT where space is very limited (see Fig. 1) especially in the forward direction. The substrate is 1.2 mm thick aluminum nitride, where each side of the HDI serves one side of the silicon wafers. The AToM chips are bonded to the flexible fanout traces after the fanouts for each side are glued to the HDI. There are 3 different

[3] Upilex™, UBE Industries Ltd, Japan.

HDI designs holding 14, 20, and 9 AToM chips for layers 1–2, 3, and 4–5, respectively.

All of the HDIs for layers 1–3 are now loaded and tested. Several have been bonded to detector-fanout assemblies. Production of the HDIs for layers 4 and 5 should be complete by the end of October, 1998.

6. The AToM chip

A detailed description of the AToM chip can be found in Ref. [11]. Here, we will review the basic features and present new test results.

Due to the 4.2 ns PEP-II bunch crossing period, the SVT front-end electronics must be able to simultaneously acquire, digitize, and readout. The AToM chip (A Time-over-threshold Machine) was designed specifically for the BaBar experiment to meet these requirements. The chip is manufactured by Honeywell[4] using their RICMOS IV radiation-hard CMOS bulk technology. Some AToM features are listed below:

- 128 channels per chip.
- Simultaneous acquisition, digitization, and readout.
- Sparsified readout.
- Time-over-threshold readout (4 bits, adjustable sample rate).
- Redundant clock, command, and readout.
- Internal charge injection for calibration (5 bit DAC, 0.5 fC/count).
- CR-RC^2 shaping with variable peaking time (100, 200, 300, or 400 ns).

The AToM chip was originally designed to operate at 60 MHz, however the chip would function only in a very narrow duty-cycle window, so we will operate the chip at 30 MHz.

The yield from Honeywell for the first lot of AToM chips was about 50%, which was lower than expected. These chips were also prone to oscillations in the amplifier. The oscillations were suppressed with two extra wire-bonds on the surface of the chip and an adjustment in the analog voltage in order to correct the biasing of the input transistor.

A second submission of the AToM chip (referred to as AToM-II) was ordered, with the biasing of the input transistor corrected, in order to safely have enough chips to complete the SVT. Preliminary results show that the AToM-II chips have higher gain and lower noise, especially at longer peaking times. The AToM-II chip will most likely be used in layers 4 and 5.

The noise and gain for the AToM chip has been measured with chips on test boards, chips mounted on HDIs bonded to detectors, and for a fully assembled module that was placed in the interaction region during PEP-II commissioning. Table 3 lists the results of some gain and noise measurements along with some preliminary noise measurements for the AToM-II chip. The noise is lower for the longer peaking times, especially for the AToM-II chip. The chips in the inner layers will use shorter peaking times due to the higher occupancy from PEP-II backgrounds. A peaking time of 400 ns will be used for layers 4 and 5 where occupancies are lower. The total ϕ-strip length for layer 5 is 26.5 cm giving a total capacitance of about 37 pF, which translates into an estimated equivalent noise charge of 1200 electrons for the AToM-II chip. While the AToM-I noise levels are higher than expected, the thresholds can still be set at four times the noise level and be well below the expected normal-incidence, minimum-ionizing signal size of about 20 000 electrons. As previously mentioned, the AToM-II chips, which have better noise performance, will probably be used in layers 4 and 5. The after-installation noise values for the module that was placed 3.3 cm from the beam during PEP-II commissioning were consistent with measurements in the lab.

Table 4 gives the estimated average noise for the SVT layers. The estimated average capacitance values include the wafer inter-strip capacitance and capacitance to the backside, fanout inter-strip capacitance and capacitance to the backside, and the capacitance from the fanout traces crossing the z-side strips. An average length was used for the z-side fanout traces. The estimated average noise ranges from 950 electrons, for the z-side of layer-1, to 1700 electrons for the ϕ-side of layer-3. The

[4] Honeywell Inc., Minneapolis, MN, USA.

Table 3
AToM-I and preliminary AToM-II gain and noise results in equivalent noise charge as measured for chips on test boards and a layer-2 module

Peaking time	100 ns	200 ns	400 ns
AToM-I gain	190 mV/fC	235 mV/fC	200 mV/fC
AToM-I noise			
Test board	450 e^- + 47 e^-/pF	375 e^- + 45 e^-/pF	325 e^- + 39 e^-/pF
Layer 2 module, ϕ-side	1350 e^-	1200 e^-	1050 e^-
Layer 2 module, z-side	1050 e^-	850 e^-	750 e^-
AToM-II noise			
Test board	375 e^- + 41 e^-/pF	300 e^- + 35 e^-/pF	225 e^- + 27 e^-/pF

Table 4
Estimated average capacitance and noise for the SVT layers

Layer	Estimated average capacitance (pF)	Chip	Peaking time (ns)	Estimated average noise (e^-)
1 ϕ	20	AToM-I	100	1400
1 z	11	AToM-I	100	950
2 ϕ	21	AToM-I	100	1450
2 z	12	AToM-I	100	1000
3 ϕ	29	AToM-I	200	1700
3 z	17	AToM-I	200	1150
4 ϕ	32	AToM-II	400	1100
4 z	29	AToM-II	400	1000
5 ϕ	37	AToM-II	400	1200
5 z	33	AToM-II	400	1100

layer-2 estimated noise values agree well with the measured values in Table 3.

Fig. 2 shows the measured Time-Over-Threshold (TOT) response as a function of injected charge for one chip. The TOT response is roughly logarithmic, giving higher segmentation for smaller amounts of charge. The response is not as good as we had hoped [11], but it will still be useful for clustering and background rejection.

Table 5 lists the AToM-I power consumption per channel. The chip uses 4.6 mW/channel, which can be handled by the cooling system.

Four AToM chips were tested after a 2.4 MRad dose of radiation from a ^{60}Co source [12]. Three of the four chips used the high-gain setting, which will be used in the experiment. One of the three high-gain setting chips was irradiated while under power. The noise and gain were measured before and after irradiation for peaking times of 100, 200, and 400 ns. For the three high-gain chips, the gain decreased from 0 to 20%. For the two chips that were not under power during irradiation, the noise with no detector capacitance increased by 40% and the noise per pF of detector capacitance increased by 25%. The increase did not seem to be correlated with the peaking time. For the one high-gain setting chip that was under power during irradiation, the noise increase for no detector capacitance was 7%. There was no increase in the noise per pF of detector capacitance. This result suggests that the p-channel MOS input transistors incur less damage when the AToM chip is powered up. More chips are currently being irradiated to check this result.

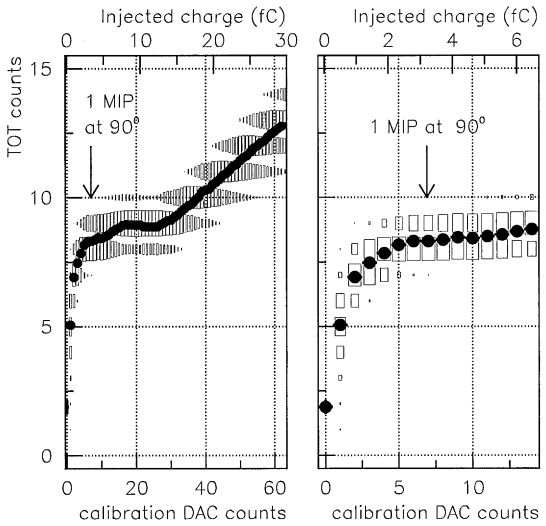

Fig. 2. Measured Time-Over-Threshold response for one AToM-I chip as a function of injected charge for a peaking time of 200 ns and a sample rate of 15 MHz. One TOT count corresponds to 67 ns. One calibration DAC count corresponds to about 0.5 fC of injected charge. The area of each box is proportional to the number of hits. Each dot is the average TOT value for that calibration DAC setting. The plot on the left shows the full calibration DAC range. The plot on the right shows up to a calibration DAC setting of 15.

Table 5
Power consumption for the three voltages needed to power the AToM-I chip

Source	Power
Digital 5 V	2.46 mW/channel
Analog 5 V	1.84 mW/channel
Analog 2.2 V	0.29 mW/channel
Total	4.59 mW/channel

7. SVT construction and assembly

Fabrication of the SVT components is nearly complete. All silicon wafers, HDI substrates, and back-end data transmission electronics are in hand, as of October 1998. All of the silicon wafers and fanouts have been assembled, bonded, and tested. All HDIs for layers 1–3 have been loaded with AToM-I chips, many of which have been glued and bonded to the detector-fanout assemblies. The first sextant (layer 1–2 module) was completed in the first week of October 1998. We anticipate that module production will be complete by the beginning of January 1999.

The support cones, cooling rings, and space-frame have been fabricated and assembled. The modules will be assembled onto the support cones from mid-November 1998 through February 1999. The SVT will be ready for installation by early March 1999.

8. Summary and conclusions

The Silicon Vertex Tracker for the BaBar experiment consists of five layers of double-sided, AC-coupled silicon microstrip detectors. The outer two layers use a novel arch-shaped design, which reduces the silicon incidence angle for tracks in the forward and backward regions. The silicon is read-out by a custom IC (the AToM chip), which simultaneously acquires, digitizes, and reads-out data.

The AToM-I chip had problems with oscillations, which were corrected with two bonds on the surface of the chip and an adjustment in the analog voltage. The noise and power consumption for the AToM-I chip are acceptable, but higher than expected. Preliminary tests of the AToM-II chip, which will be used in layers 4 and 5, indicate that it has higher gain and lower noise, especially at longer peaking times.

After gluing and bonding the fanouts to the silicon, the fraction of bad channels per detector-fanout assembly ranges from 2–4%. Pinholes are the largest single contribution to the number of bad channels. Each wafer has an average pinhole fraction of about 1% per side.

Our current schedule shows that the SVT will be ready for installation in March 1999.

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