The BaBar Silicon Vertex Tracker (SVT)

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Outline

• Requirements
• Detector Description
• Performance
• Radiation
SVT Design Requirements and Constraints (from TDR)

**Performance Requirements**
- $\Delta z$ resolution < 130 $\mu$m
- Single vertex resolution < 80 $\mu$m.
- Stand-alone tracking for $P_T < 100$ MeV/c.

**PEP-II Constraints**
- Permanent dipole (B1) magnets at +/- 20 cm from IP.
  - Polar angle restriction: $17.2^\circ < \Theta < 150^\circ$.
  - Must be clam-shelled into place after installation of B1 magnets.
- Bunch crossing period: 4.2 ns (nearly continuous interactions).
- Radiation exposure at innermost layer (nominal background level):
  - Average: 33 kRad/year.
  - In beam plane: 240 kRad/year.
- SVT is designed to function in up to 10 X nominal background.
SVT characteristics

- Five layers, double sided
  - Barrel design, L4 and 5 not cylindrical
  - 340 wafers, 6 different types
  - Low mass Kevlar-Carbon Fiber support ribs
- Upilex fanouts to route signal to ends
- Double-sided AlN HDI (104 of these)
  - Outside tracking volume
  - Mounted on Carbon Fiber cones (on B1 magnets)
- Atom chips
  - 1156 chips, 140K channels
<table>
<thead>
<tr>
<th>Layer</th>
<th>Radius (mm)</th>
<th>Modules/</th>
<th>Wafers/</th>
<th>( \Phi \text{Pitch} ) (( \mu \text{m} ))</th>
<th>Z Pitch (( \mu \text{m} ))</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>32</td>
<td>6</td>
<td>4</td>
<td>50 or 100</td>
<td>100</td>
</tr>
<tr>
<td>2</td>
<td>40</td>
<td>6</td>
<td>4</td>
<td>55 or 110</td>
<td>100</td>
</tr>
<tr>
<td>3</td>
<td>54</td>
<td>6</td>
<td>6</td>
<td>55 or 110</td>
<td>100</td>
</tr>
<tr>
<td>4a</td>
<td>124</td>
<td>8</td>
<td>7</td>
<td>100</td>
<td>210</td>
</tr>
<tr>
<td>4b</td>
<td>127</td>
<td>8</td>
<td>7</td>
<td>100</td>
<td>210</td>
</tr>
<tr>
<td>5a</td>
<td>140</td>
<td>9</td>
<td>8</td>
<td>100</td>
<td>210</td>
</tr>
<tr>
<td>5b</td>
<td>144</td>
<td>9</td>
<td>8</td>
<td>100</td>
<td>210</td>
</tr>
</tbody>
</table>
Space Frame and Support
Cones...mounted on B1 magnets
SVT Modules

Z-Side
- High Density Interconnect (mechanical model)

Phi-Side
- Flexible Upilex Fanout
- Micro-bonds
- Si Wafers
- Carbon/Kevlar fiber
- Support ribs

Fanout Properties:
- $< 0.03 \% X_0$
- 0.52 pF/cm
SVT High Density Interconnect

**Functions:**
- Mounting and cooling for readout ICs.
- Mechanical mounting point for module.

**Features:**
- AlN substrate.
- Double sided.
- Thermistor for temp. monitor.
- 3 different models.
Silicon Wafers

Features
• Manufactured at Micron.
• 300 µm thick.
• 6 different wafer designs.
• n⁻ bulk, 4-8 kΩ cm.
• AC coupling to strip implants.
• Polysilicon Bias resistors on wafer, 5 MΩ.

Bulk Properties
• Bias current: 0.1 to 2.0 µA
• Bulk current: 0.1 to 2.0 µA
• Depletion voltage: 10 to 45 V

Strip Properties

<table>
<thead>
<tr>
<th></th>
<th>n-side</th>
<th>n-side</th>
<th>n-side</th>
<th>p-side</th>
</tr>
</thead>
<tbody>
<tr>
<td>Strip Pitch</td>
<td>50 µm</td>
<td>55 µm</td>
<td>105 µm</td>
<td>50 µm</td>
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<tr>
<td>Inter-strip C</td>
<td>1.1 pF/cm</td>
<td>1.0 pF/cm</td>
<td>1.0 pF/cm</td>
<td>1.1 pF/cm</td>
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<tr>
<td>AC decoupling C</td>
<td>20 pF/cm</td>
<td>22 pF/cm</td>
<td>34 pF/cm</td>
<td>43 pF/cm</td>
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<tr>
<td>Implant-to-back C</td>
<td>0.19 pF/cm</td>
<td>0.36 pF/cm</td>
<td>0.17 pF/cm</td>
<td></td>
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<tr>
<td>Bias R</td>
<td>4 to 8 MΩ</td>
<td>4 to 8 MΩ</td>
<td>4 to 8 MΩ</td>
<td>4 to 8 MΩ</td>
</tr>
</tbody>
</table>
Silicon Wafers

- Bias ring
- Polysilicon bias resistor
- p^+ Implant
- Al
- Edge guard ring
- P-stop
- n^+ Implant
- Polysilicon bias resistor
- Edge guard ring

p^+ strip side

n^+ strip side

50 \mu m

55 \mu m
The AToM Chip

Custom Si readout IC

AToM = A Time Over threshold Machine

Features:

• 128 Channels per chip
• Rad-Hard CMOS process (Honeywell)
• Simultaneous
  – Acquisition
  – Digitization
  – Readout
• Sparsified readout
• Time Over Threshold (TOT) readout
• Internal charge injection
The AToM Chip

**Amp. Shape. Discr. Calib**
- 5-bit CAL DAC (0.5 fC/count)
- 5-bit Thr DAC (0.05 fC/count)
- Shaping time 100 - 400 ns
- Typical threshold 0.6-0.9 fC

**Trigger Latency Buffer**
- 15 MHz Sample rate
- Total storage = 12.7 us

**TOT. Tstamp. Buffering**
- 4 bits TOT (logarithmic)
- 5 bits Hit Tstamp (67 ns/count)
- 4 buffers / channel
Performance

- Calibration, Noise
- Occupancy
- Efficiency
- Intrinsic Resolution
Calibration

- Noise, gain, pedestals, bad channels obtained from scanning threshold with and without charge injection and counting hits
  - 600K errfun fits, 150K linear fits
  - once a day; takes ~ 2 minutes
- Very stable
- Downloadable chip parameters have not changed since Oct 1999
1 MIP at normal incidence, about 23,000 electrons
Occupancy (Layer 1)

Offline $\Delta t \sim 300$ nsec
$\rightarrow$ effective occupancy lower by factor $\sim 3$
Cluster efficiency

$\varepsilon \sim 97\% \quad (SW + HW)$

Excluding 9/208 malfunctioning readout sections
Resolution

Resolution vs projected angle - Zed

SVT Hit Resolution vs Angle - Zed View
Standalone reconstruction of low $P_T$ tracks

Reconstruction of $\pi_s$ from $D^* \rightarrow D \pi_s$ is (mostly) with SVT alone.
Map of malfunctioning modules (9/208)

- Layer 1 perfect
- Problems are from
  - shorts on hybrids
  - elec. problems on wafers
  - slipped out cables

FORWARD

BACKWARD
Radiation

- Monitored by 12 diodes at ~ radius of layer 1
- Diodes can abort beam
- Operation tricky due to heavy radiation damage
Measured absorbed Dose

Graph showing the measured absorbed dose over the year 2001, with different lines representing different measurement points (Non-MID-plane, BW-MID Inner, and FE-MID Outer).
Projected absorbed dose, midplane

Based on PEP II current profile and measured dose/current

Includes injection, etc

A bit conservative....

Off-midplane ~ x5 lower
Consequences of high doses

• Bulk damage to Si
  - increase $I_{\text{LEAK}}$ → increase in noise
    • not a real problem until very high doses
  - type inversion

• Damage to chips
  - originally tested (fully) only to 2 MRad
  → test to higher doses
Bulk Damage

NIEL scaling: high energy electron cause significant damage (~1/10 of hadrons)

Not appreciated by us until recently
Tests at Elettra (Trieste)

- $C^{-2}$ vs $V$ curve show inversion
- Results in ~ agreement with NIEL scaling hypothesis
- Leakage current increase of order $2 \mu A/cm^2$
  - agrees with in-situ measurement
Detector Radiation Tests (Cont.)

- Electrical properties after inversion:
  - Strip isolation OK
  - Edge currents, no sudden increase, manageable
- Still to do: test of charge-collection efficiency
  - According to literature, should be OK
  → sensors OK to at least 5-6 MRad
AtoM tests beyond 2MRad

Noise = $\alpha + \beta C_{\text{Load}}$

Significant increase in noise but chip functions to at least 5 MRad
SVT Module Replacement

- Summer 04 shutdown: replace
  - L1/2 midplane modules
    - worst case dose by then ~ 3.5 MRad
  - other malfunctioning modules
- New modules identical to existing ones
- New modules under construction now
Conclusion

• The BaBar SVT is working well
  - efficient
  - resolution according to spec
  - standalone tracking
• Replace radiation damaged modules in 04
• Extend lifetime to ~ 07
• After that?
  - depends on many things (machine, physics etc.)