



# Tracker Outer Barrel Silicon

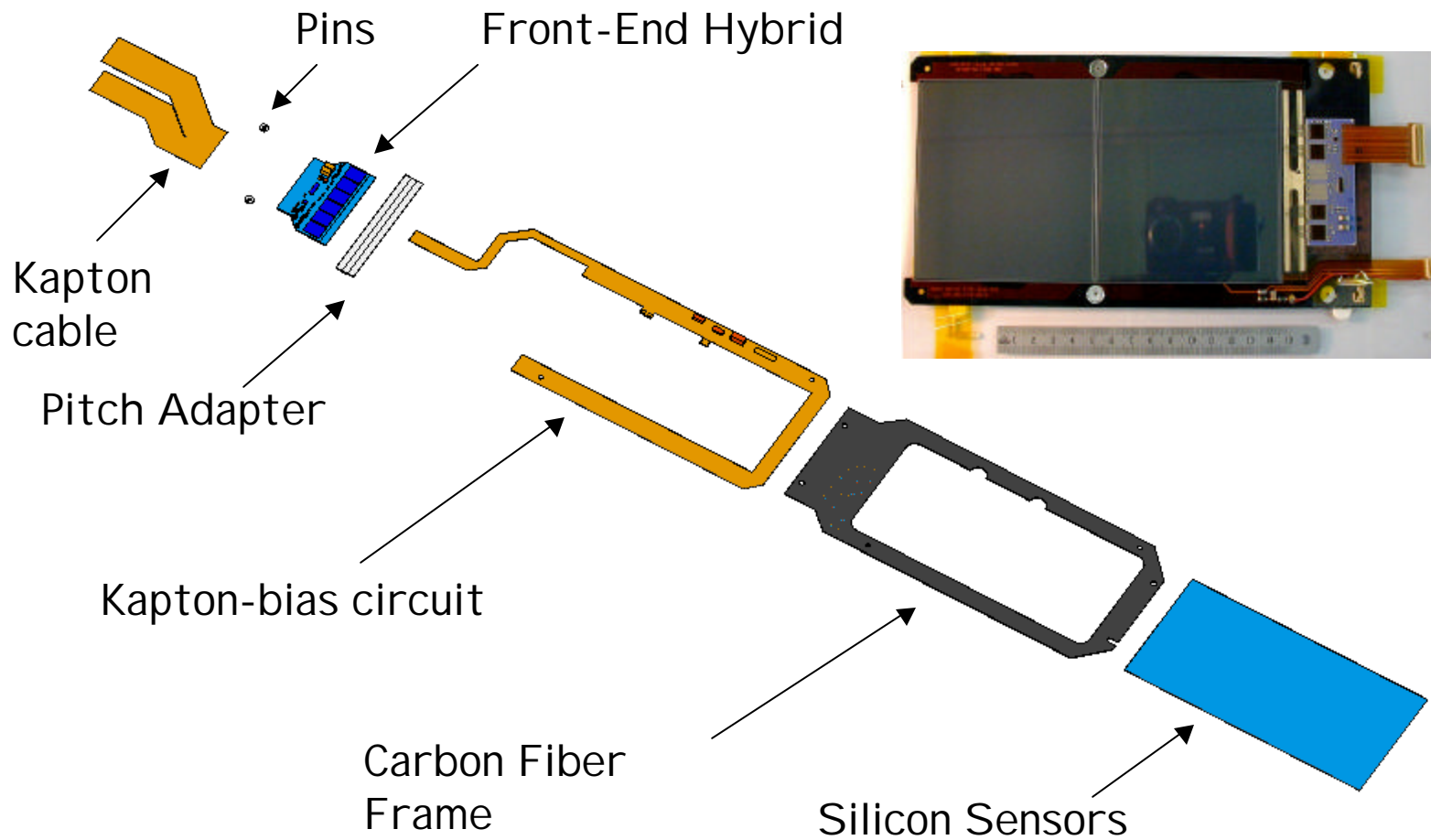
*Slawek Tkaczyk*

*Fermilab*

*US CMS Silicon Tracker Project*

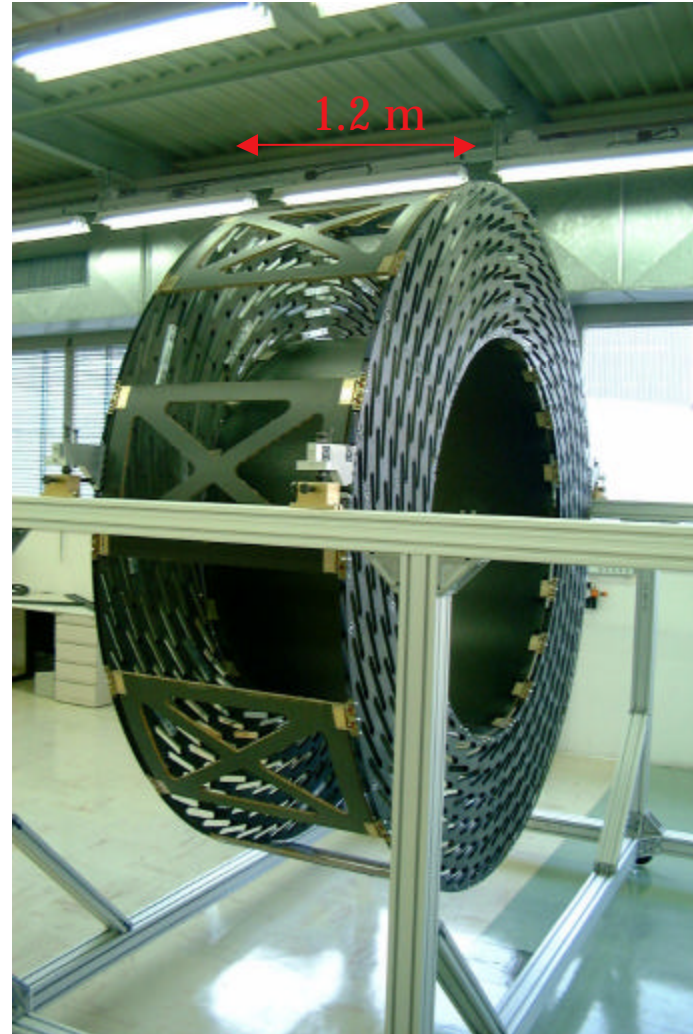
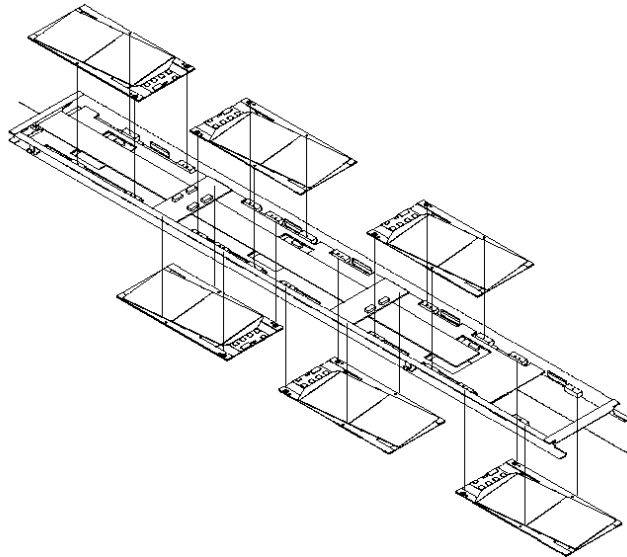


# Module Components



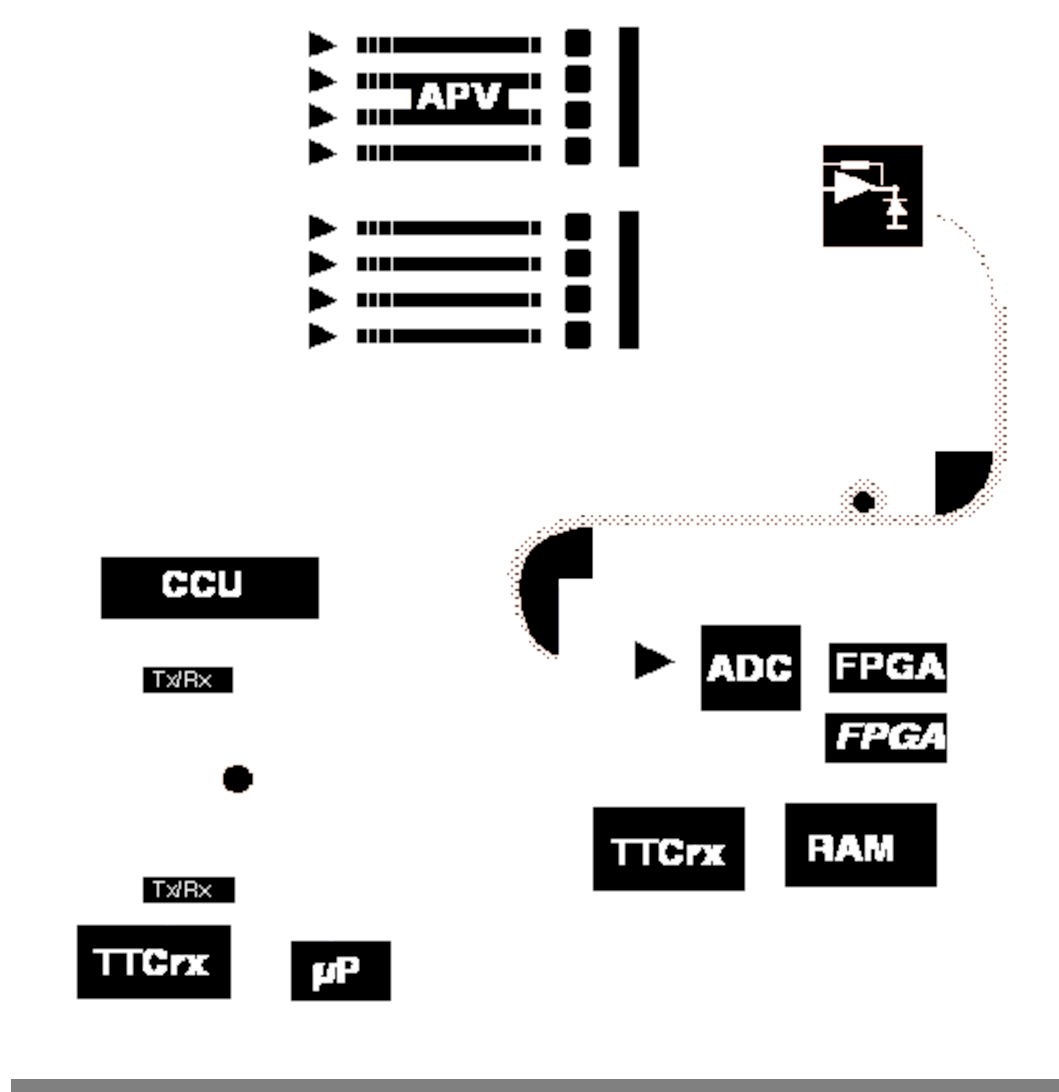


# Rods





# Tracker Readout System



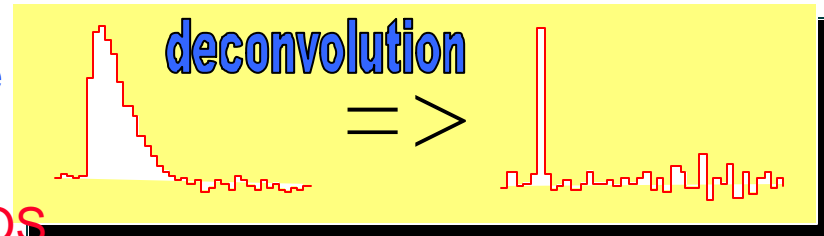


# APV History

## Pre-history

- 1991... RD20 & deconvolution principle

1992 CMS LoI



## 1.2 $\mu$ m Harris AVLSIRA radiation hard CMOS

- 1993 - APV3 - 32 channel pipeline chip implementing CR-RC shaping and 3-weight deconvolution signal processing

1994 CMS TP

- 1995 - APV5 - 128 channels with addition of analogue multiplexer
- 1996 - APV6 - 128 channels with analogue multiplexer, bias generator, calibration control, and I<sup>2</sup>C interface. Full CMS read-out functionality.
- 1998 - Development of APV6 into MSGC read-out chip, APVM

1998 CMS Tracker TDR

## 0.8 $\mu$ m DMILL radiation hard CMOS

- 1997-99 - APVD - development of DMILL versions

## 0.25 $\mu$ m CMOS

- 1998-2000 - development of APV25

1999 CMS all-silicon Tracker



## Critical Path Items

- The Si-Tracker group is presently evaluating a recently discovered feature of the APV25.
- The 'feature' manifests itself in two related ways - see the next few slides.
- It is very unlikely that the APV25 will be re-designed at this point.
- A test beam study in mid-May should hopefully resolve the remaining concerns-data analysis in progress.
- **These higher order concerns should in no way detract from the otherwise superb performance of the APVs.**



Four chip TOB hybrid



# HI Ps and Pinholes

## HI Ps

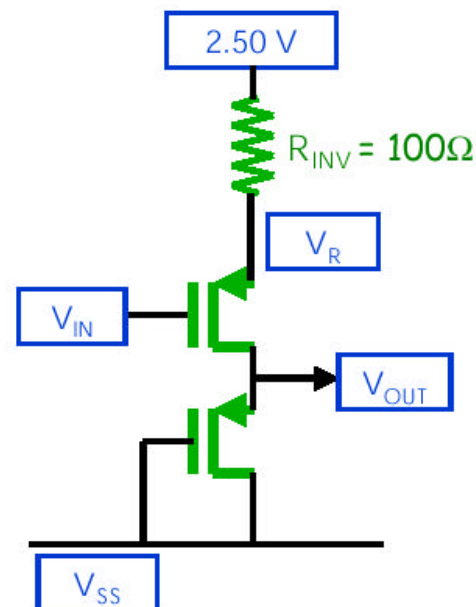
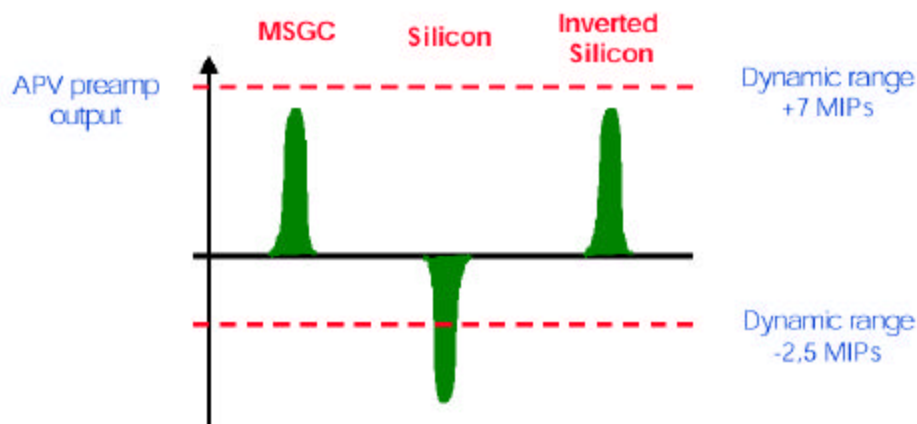
- Highly Ionizing Particle (1000X minimum ionizing) resulting from nuclear interactions in the silicon.
- These are rare events.
  - $3.9 \times 10^{-4}$  per 500 $\mu$  layer per incident pion.
- Rates confirmed in the recent exposure in the PSI test beam
- HIPs lead to large signals on a few strips.
  - This can saturate (disable) the entire APV (128 channels) for ~200 ns.

## Pinholes

- Detector strips are capacitively coupled to the APV.
- The capacitors can occasionally be shorted (pinhole).
  - Leads to a DC current **into** the APV.
  - If enough pinholes are present the APV will be **permanently** disabled (until the pinholes are removed).



# MSGC Legacy



- ❖ **Big signal from silicon (holes) gives -ve pulse at  $V_{IN}$ :**
  - Inverter FET switches hard on, which steals current from 127 other inverters. (APV disabled until capacitor discharges.)
  - N.B. If  $R_{INV}$  were reduced, total current available to inverters would increase.

- ❖ **Leakage current via pinhole into APV :**

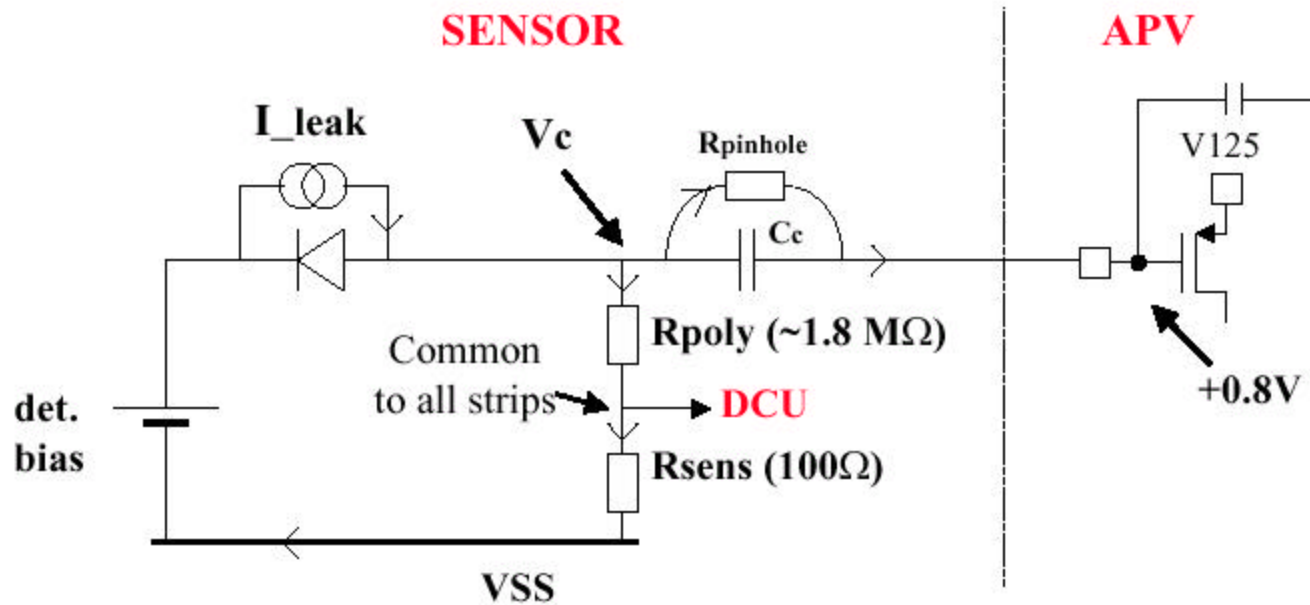
- Same again, but permanent.

- ❖ **Leakage current via pinhole out of APV :**

- Inverter FET switches hard off. Takes no current, so other 127 channels still work.



# Bias Circuit



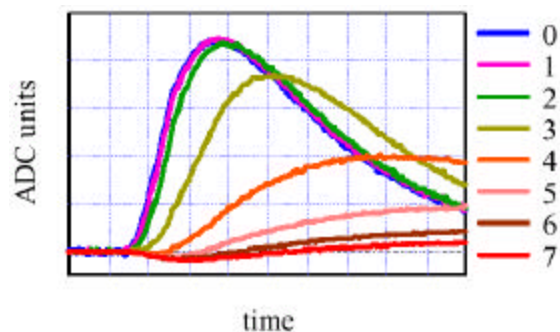
If  $V_c > 0.8$  Volts, current flows into APV via pinhole (BAD).  
If  $V_c < 0.8$  Volts, current flows out of APV via pinhole (OK).

$V_c$  will exceed 0.8 V in old (irradiated) detectors with large leakage current.



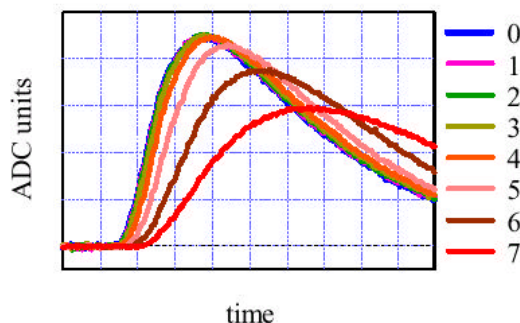
# Number of Pinholes

Inject  $1 \mu\text{A}$  of (pinhole leakage) current into 1-7 APV channels.  
Then inject a 1 MIP charge into 1 other channel and see what it looks like:



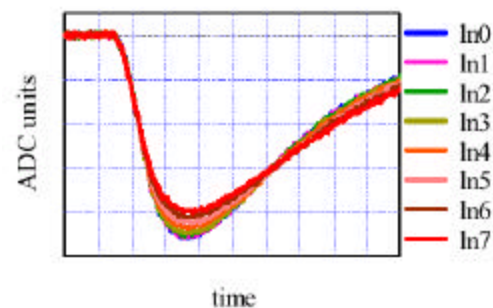
$R_{\text{inv}} 100 \Omega$

**Signal suffers if more than 2 pinholes**



$R_{\text{inv}} 50 \Omega$

**Signal suffers if more than 4 pinholes**



APV inverter off

**Signal OK for more than 7 pinholes (but reduced dynamic range)**



## APV Concerns in Perspective

- Both HIP events and pinholes (after installation) are very rare.
  - CDF and D0 Run IIa: “A few pinholes”.
- Both problems can be mitigated by changing  $R_{inv}$  from 100 to 50 ohms.
- In cases where there are more than 4 pinholes per APV the inverter can be turned off (with loss of dynamic range).
- It may be possible to avoid the pinhole effect by applying a small voltage to the bias ‘ground’.
- The test beam activity at PSI in 15-21 May 02 confirms the understanding of the HIP effect.



## FE hybrid status

- Industrial hybrid (V0 – unpackaged chips on thick film ceramics) production started with two producers. Over 160 hybrids delivered by one vendor (yield 65%).
  - A lot of little problems in manufacturing or final assembly (“the feature size” is too small for mass production; difficult cable attachment).
- The 2<sup>nd</sup> producer had problems with shorts – a handful delivered.
- (V1) Design of this version of the hybrid (packaged chips on ceramic) is done. Order will go to 1<sup>st</sup> producer after delivery of the 160(x0.65) hybrids
- (V2) 40 hybrids of this type (packaged chips on FR4) were received in Strasbourg. 10 have been populated and they look okay.
  - Robust media but needs to be evaluated –e.g. thermal issues



## Hybrid- New Technology Decision

- New Candidate Technology: monolithic FR4 (kapton cable is part of the hybrid)
- At the next CMS Week in June '02 the technology will be chosen
- Issues to be addressed by June are:
  - Mounting scheme: should hybrid be glued on a rigid substrate (CF or graphite) before adding pitch adapter;
  - Radiation hardness;
  - Electrical performance;
  - Thermal performances;
  - Price;



## Hybrid- Delivery Schedule

- Decision expected in June'02
- 10-20 FR4 prototypes being done
- It takes 6 months from the decision 'till deliveries of first production FR4 hybrids (bidding, order placement, fabrication, etc.)
- First hybrid from production order expected in Jan'03
- A short order (~1000) will be placed after positive decision resulting in hybrids delivered in October '02.



# Status of Component Orders

- Sensors: Contracts signed
- Frames: Tender finished
- Pitch Adapters: Market Survey (MS) done, Small orders done/prepared
- APV25 Chips: small fraction available
- Other ASICS (PLL, MUX, DCU): being packaged
- FE Hybrids: Technology decision imminent....
- Optoelectronics: Tenders (4) finished and LOI sent for some contracts



# Module Testing at SiDet



**ARCS (2/7)**



**CMS DAQ (3/4)**

Two PC-based test systems are now in operation at SiDet. The DAQ system represents a pre-prototype version of the final system.



# Rod Testing

- Plan is to perform module burn-in once rods are assembled
  - We are studying use of commercial chest freezers and commercial chillers for the burn-in facility
  - We're in discussion with CERN physicists and engineers to specify the thermal-cycling tests to be done during burn-in.
  - This will drive the design of the cooling and controls.
- We hope to prototype much of the system this summer/fall.



## Conclusions

- The U.S. CMS Si-Tracker effort is part of a larger effort to build the CMS Tracker system.
- Our project relies on timely deliveries of quality components from European collaborators and assemble these into modules and rods.
- Viability of the final APV25 + hybrid designs are being finalized.
- The first news from the Test Beam look promising.
- The current schedule has us starting production in early 2003.