Assumptions

- Electrical and optical hybrids not burnt-in prior to arrival at UCSB/FNAL
  - → No burn-in program for foreseen before full production
- Rod components currently scheduled to arrive much later than module components (~6 month)
  - → Large supply of finished modules prior to rod construction
  - → Minimal information of long-term stability of most components
    - – Necessitates burn-in of a fraction of modules prior to rod construction

      Sample each construction jig periodically
- Vienna cold box and rod burn-in only systems viable for such a program
  - → Vienna cold box software already tested and written

UCSB Short-term Testing Plan

- Characterize hybrid (+PA) on arrival
  - → Basic functionality and deep test (ARC)
    - – Specific bad channel requirements for hybrid (+PA)
- Re-characterize module on completion of construction
  - → Basic functionality, deep test, IV curves (ARC)
    - – Different bad channel requirement for module
- Vienna cold box test fraction of modules (DAQ)
  - → Acts as ~24 hour module burn-in
    - – Scaled bad channel requirements for change in gain, grounding, etc.
    - – Identifies mechanical/bond/electrical weaknesses prior to production of large number of modules
    - – Reduces reworking of rod/retrofitting of modules

Deep Test Modifications

- Make bad channel requirements specific to component type tested
  - → (hybrid, hybrid+PA, module)
- Remove/loosen relative percentage/sigma requirements
- Tighten/add fixed requirements
- Motivate requirements on silicon tracker performance

Pedestal/Noise Test

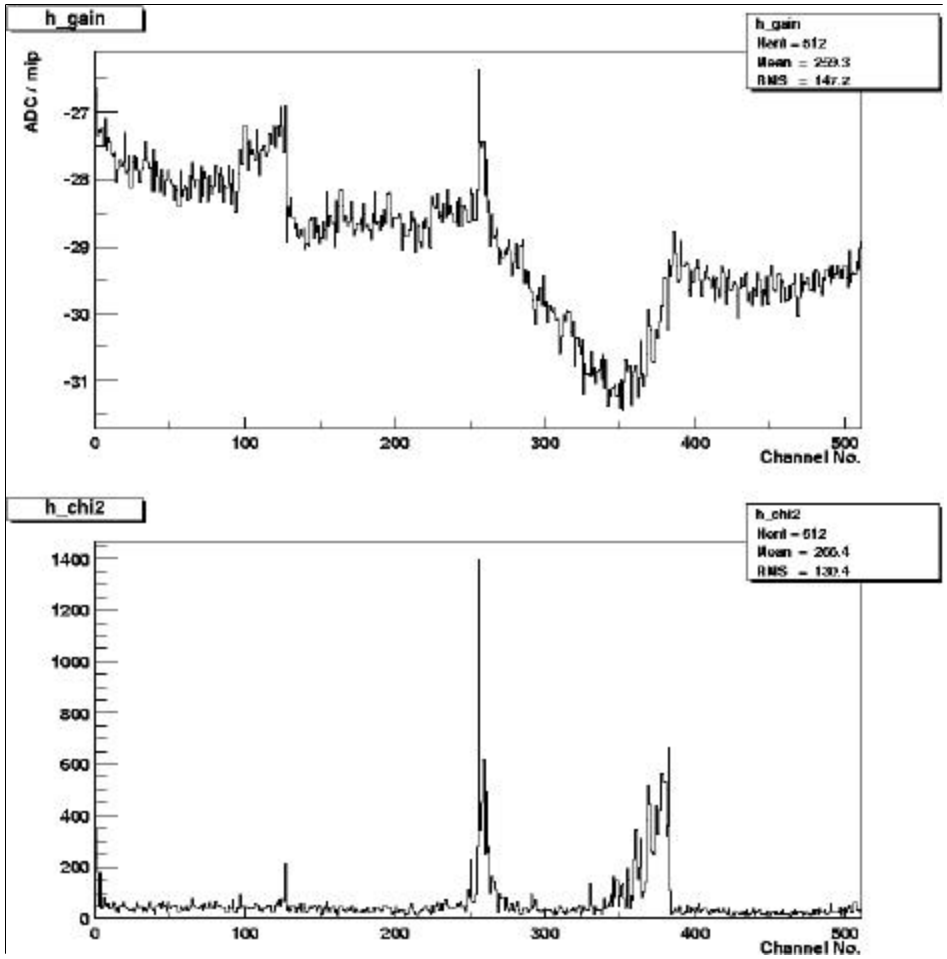
- Increase minimum noise test
  - → Fractional requirements too wide to discern saturated/dead FE preamplifier
- Replace fractional pedestal requirements with $|P_i - P_{chip}| < P_{cut}$
  - → P_{cut} motivated by decrease in dynamic range of channel
- Special requirements on chip edges if necessary

Pulse Shape Test

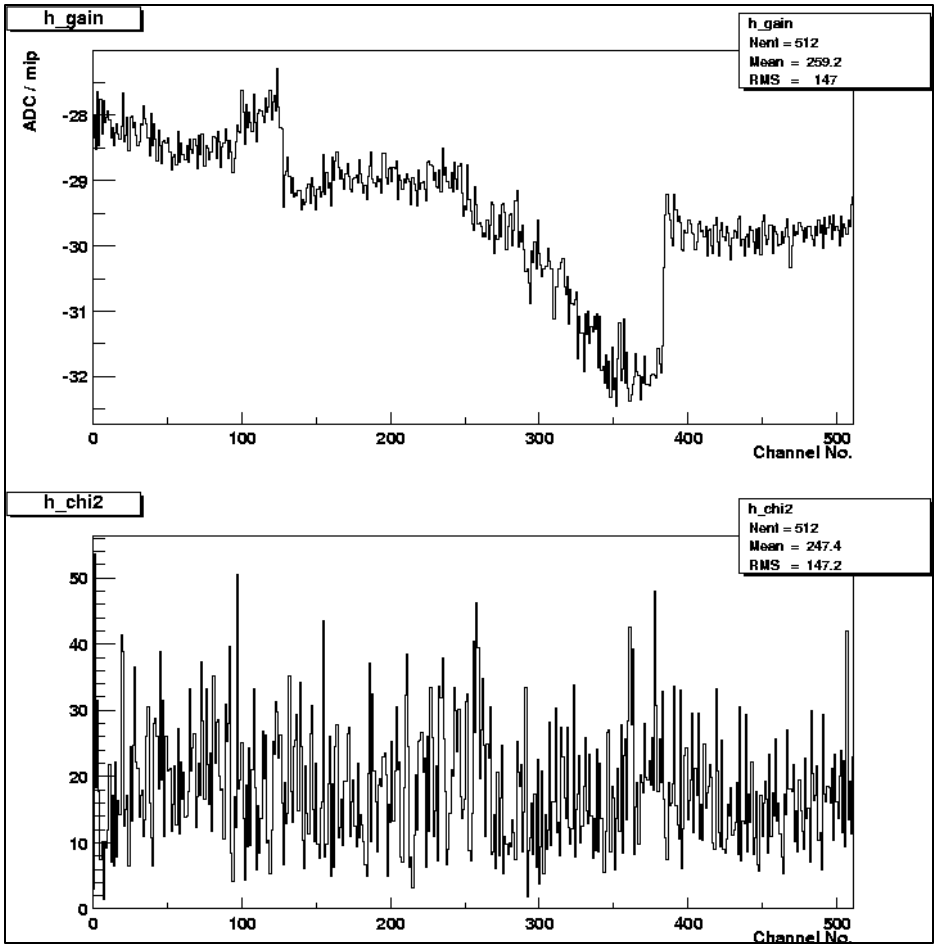
- Remove current pulse shape requirements
  - → Include rise-time/fall-time/peak-time requirement
- Replace pulse shape with gain measurement
  - → Measure pulse heights at 6-13 calibration injection setting between 0-3 MIPs and fit
  - → Require gain between G_{low} and G_{high}
    - – Gain uniformity specification

      Calibration circuit may not be uniform
  - → Require $\chi^2<\chi^2_{cut}$ (χ^2 based on noise measurement)
    - – Finds non-linear charge response and gain non-uniformities
- Should be relatively simple to include in ARC software
- See following example

Hybrid Gain Measurement(1)



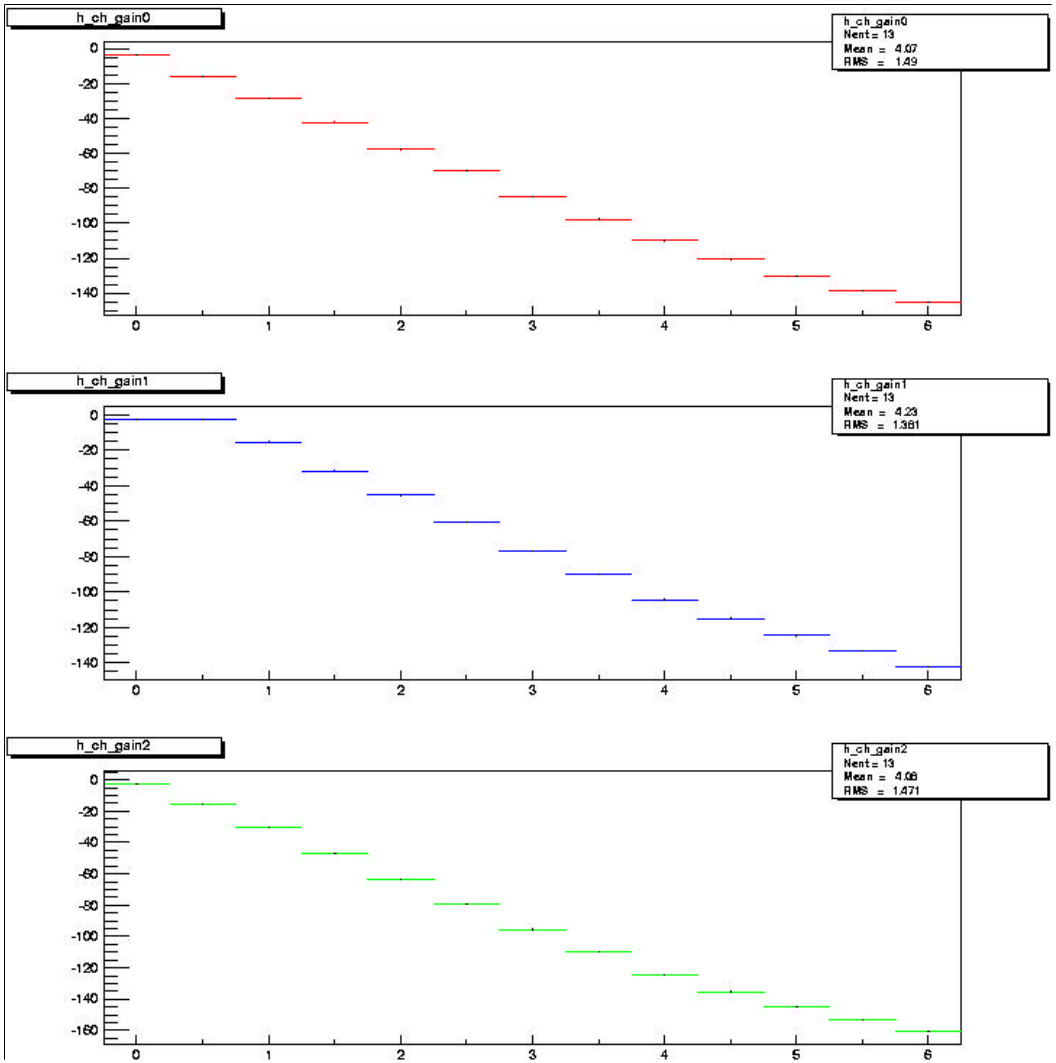
0-3 MIPs



0.25-3 MIPs

Hybrid Gain Measurements(2)

- Three channels' pulse height vs. MIP injected
  - → First 'regular'
  - → Second 1st channel of chip 3
  - → Third 63th channel of chip 3
- Gain non-uniform and bad χ^2 if 0 MIP point included for chip 3
- Improved if 0 MIP excluded
- Mostly likely calibration circuit non-uniformities



Pipeline Test

- Add pipeline capacitor pedestal/noise requirement
  - → Widen relative to channel requirement according to decreased statistics
- Add pipeline column pedestal/noise requirement
- Remove bad capacitors/columns from channel pedestal/noise calculation

Ladder Grading

- Grade ladders by fraction of bad capacitors
  - → Bad channel=190 capacitors
  - → Bad column=128 capacitors
- Treat chip edges differently (if necessary)

Necessary Infrastructure

- DAQ with 10 hybrid channels
- LV/HV power supplies
  - → Reusable for rod burn-in
- Vienna cold box
- DI/O PC board
- 1.5 kW chiller
- Module carriers