Available on CMS information server

CMS NOTE 2001/046

The Compact Muon Solenoid Experiment

CMS Note

Mailing address: CMS CERN, CH-1211 GENEVA 23, Switzerland

15 October 2001

A Test Setup for Quality Assurance of Front End Hybrids

M.Axer, F.Beissel, C.Camps, V.Commichau, G.Fluegge,
T.Franke, K.Hangarter, C.Ilgin, J.Mnich, J.Niehusmann,
M.Poettgens, P.Schorn, R.Schulte, W.Struczinski

III. Physikalisches Institut B, RWTH Aachen, Physikzentrum Aachen, D-52056 Aachen, Germany

Abstract

The APV Readout Control (ARC) Test Setup is a compact, cost efficient test and diagnostic tool which is suited for full operation and characterisation of FE hybrids and Si-Detector modules. This note gives an overview of the construction and the features of the test facility. Based on the ARC setup and the experiences gained with one prototype FE hybrid, possible quality assurance scenarios for short and long term tests of FE hybrids are also presented.

1 Introduction

The CMS Silicon Strip Tracker (*SST*) will instrument the central region of the CMS experiment. It will be composed of four parts: the Tracker Inner Barrel (*TIB*), the Tracker Outer Barrel (*TOB*) and two Tracker End Caps (*TEC*). About 15200 silicon micro strip detector modules are foreseen to equip the SST constructing the largest all-silicon tracker in the world. One individual silicon detector module essentially consists of three elements, a set of silicon sensors, a mechanical support structure and the front end electronics (*FE hybrid*).

The construction of the SST involves a large number of industrial companies and research institutes from many different countries. The mass manufacture phase of the silicon detector modules needs an appropriate testing chain. The module production and assembly period will span over two and a half years, during which time it is essential to guarantee a simple and reproducible assembly and testing procedure among different testing centres. This means that throughout the whole production a lot of different quality assurance tests have to be performed to avoid expensive production failures. Due to the restricted manufacture time and the large number of modules to be produced, automation of testing procedures and traceability of data are mandatory. Therefore a significant number of testing environments have to be designed and distributed to all test centres within a short time period. A test facility has to fulfil the following hardware and software requirements: inexpensive structures, flexible design, user friendly operation, data handling (database access) and reproducible results.

The test facility which will be introduced here is particularly intended for diagnostic testing and quality assurance of FE hybrids. The concept provides a very compact and flexible structure. This low cost test setup evolving in Aachen is called *APV Readout Controller* (*ARC*). It provides complete control of the hybrid and all its ASIC chips. The basic functionality originates in the prototype synchrotron radiation detector (PSRD) readout setup [1] for the AMS experiment[1)] developed by some of the authors in collaboration with the ETH Zurich.[2)] An individually designed LabVIEW application called *APV Readout Controller Software* (*ARCS*) serves as a userfriendly graphical user interface which allows an easy implementation of automatic test procedures. Further information concerning the ARC system and the latest versions of ARCS can be found in [2].

2 Overview of the ARC System

2.1 Features of the Hybrid Test Setup

A fully assembled FE Hybrid is a multilayer ceramic board carrying 6 or 4 analogue readout ASICs, the APV chips [3], and two control ASICs, the PLL/MUX [4, 5] and the DCU chips [6]. An APV possesses 128 analogue channels, each composed of a low noise high gain charge sensitive amplifier and a 192 columns deep analogue buffer running at 40 MHz. The MUX/PLL chip is a combination of two chips performing the following tasks: the MUX part is intended for the multiplexing of two APV analogue output lines into one analogue data stream while the clock and the readout trigger signals are received and distributed by the PLL part. The third type of ASIC, the DCU, monitors biases and temperatures of the detector and the hybrid itself. The hybrid is biased at +2.5 V, +1.25 V and 0 V with a total power consumption of less than 3 W.

For mass production approximately 15200 fully assembled FE hybrids plus 5–10 % spares are foreseen [7]. Two types of multilayer boards have to be manufactured differing mainly by their physical dimensions (one type for TOB and TEC and another type for TIB). Corresponding to three different TOB, TIB and TEC hybrid cables three different connectors to the readout structures are needed.

The FE hybrid will play a central role within the readout and trigger chain of the CMS detector. Therefore a thorough test (functional and mechanical) of each hybrid foreseen for installation into the tracker is essential. The final conception of a functionality controling procedure will depend on experience gained on a larger number of tested hybrids, but there are some general features a reasonable hybrid test facility has to provide:

- I^2C protocol communication check with all ASICs,
- measurements of characteristics of the APV readout chip including pedestal and noise measurements, gain and pulse shapes (in peak and deconvolution mode),
- measurements of characteristics of the PLL/MUX chip and the DCU chip,

1) The Alpha Magnetic Spectrometer will be housed on the international space station.

2) We thank AMS and specially the ETH Zurich for the permission to use some of their components.

- control and measurements of the hybrid power consumption,
- functionality for long term stability tests (with and without temperature cycling).

2.2 Description of the Hybrid Test Setup

Figure 1 gives a schematic overview of the hybrid test setup intended for functionality tests developed in Aachen. A detailed description can be found in [2]. The basic concept allows the operation of two hybrids connected to one ARC board (*single board setup*) or alternatively more than two hybrids in a *multi board setup*. As indicated in the block diagram a multi board setup is composed of a number of ARC boards housed in a 19” crate connected via an extension bus for synchronisation purposes. In this case one ARC board acts as a master and the others act as slaves.

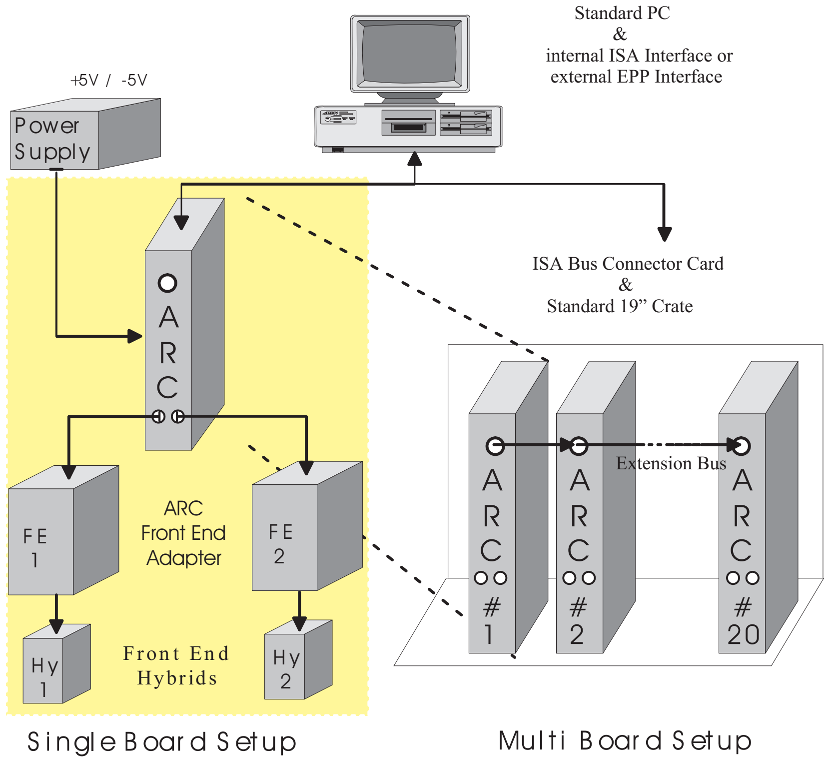

Figure 1: A simple block diagram of the hybrid test setup.

The test facility is composed of the following elements: A standard PC (minimum required equipment: CPU with 500 MHz, 128 MB RAM [3] and at least one ISA slot) operates as control device and is connected to the ARC board via a 50 pin flatcable and a PCMIO interface [8]. The PCMIO card fits into an IBM XT slot and serves as interface between the ISA bus and the ARC board. Alternatively it is possible to use the PC LPT port as an interface to connect ARC to the PC.[4]. In this case an external EPP interface [9] has to replace the PCMIO card in the setup. This allows to use a notebook as control computer resulting in a fully portable system.

A single ARC board is powered by an external, simple ± 5 V DC low voltage device and is suited for a simultaneous access and test of two FE Hybrids via one Front End Adapter (*ARC FE*) for each hybrid. For multi board setups up to twenty ARC boards are inserted into a standard 19” crate. In this case the power is delivered through the backplane 64 pin connector by the crate itself. The connection to the PC (ISA or EPP interface) is provided by a special ISA bus connector card which supplies the boards with all necessary inputs.

Details of the various components of the ARC system are given in the following sections.

[3] This is based on software (LabVIEW 6i) requirements.

[4] It is mandatory that the LPT port provides the standard *E*nhanced *P*arallel *P*ort protocol. Data sampling will be slower by a factor of two compared to the PCMIO interface.

3 The APV Readout Controller ARC

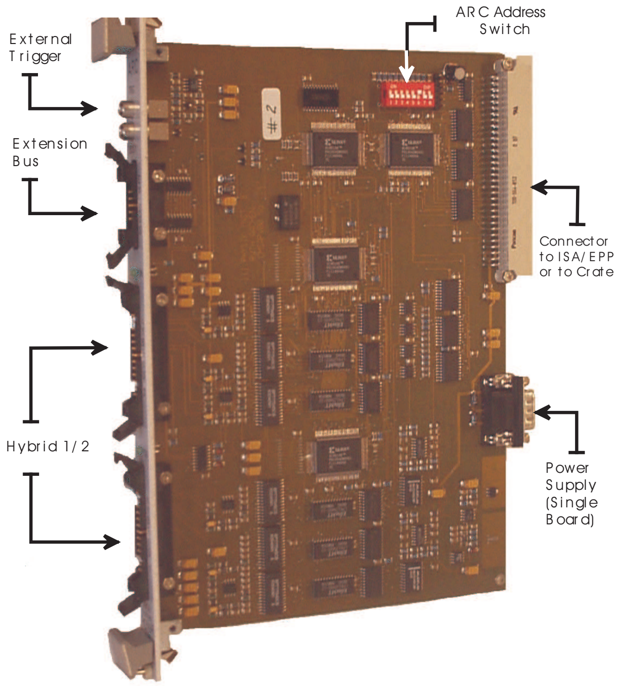

Figure 2: The APV Readout Controller [10].

A photograph of the APV Readout Controller (ARC) is shown in figure 2. The ARC is a printed circuit board designed in *Standard Double Euro Format* conforming to the specifications listed in table 1. Further details regarding the circuit description are given in [10].

There are three main function blocks on the ARC board for the operation and test of FE hybrids. These blocks are:

- clock and trigger,
- data sampling and
- slow control and low voltage control.

The properties of the three function blocks are selectable by software. This means that an operator has software access to the settings of an individual ARC board. Each board has a selectable address which is used for communication (see ARC address switch in figure 2). This address distinguishes the ARC boards within a multiple board setup.

3.1 Clock and Trigger

The clock and trigger controller located on the ARC board generates the clock and trigger signals for both hybrids. The clock itself is generated by a crystal oscillator. A software trigger or an external (NIM) generated asynchronous trigger (see external trigger connector in figure 2) is latched and finally synchronised with the system clock. Initialised by this synchronised trigger a progammable APV trigger pattern is send to each FE hybrid. All possible APV trigger patterns (RESET, CALIBRATION REQUEST, EVENT TRIGGER) are generated this way. The trigger signal can be distributed to the APVs either by a separate trigger link or as missing clock pulses.

3.2 Data Sampling

Two groups of three 8 bit FADCs–one group for each hybrid–sample the APVs analogue data with a synchronised clock (40 or 20 MHz). For correct sample timing the FADC clock phase can be shifted in 10 steps of approximately 1.7 ns. The digitised data are stored in an 8 kByte RAM for each channel.

Type	Function	Comment
Clock	internal 40 MHz	software selectable
	or external clock input	LVDS up to 40 MHz
	clock output	LVDS
Trigger	input internal	software
	input external	NIM or LVDS
	output	LVDS
Hybrid I/O	analogue inputs	6 differential voltages
	resistance	50 Ohm
	slow control	3 standard buffered I^2C links
	clock/trigger	2 LVDS clock lines
		2 LVDS trigger lines
Expansion Port	input or output	clock: LVDS
		trigger: LVDS
		synchronized: trigger LVDS
		APV trigger: LVDS
Power Requirements	1.4 A @ +5 V	
	60 mA @ -5 V	

Table 1: Specifications of the APV Readout Controller.

3.3 Slow Control and Low Voltage Control

There are three I^2C controllers [11] located on the ARC board. Two of them are used for hybrid slow control purposes (one controller for each hybrid) providing the communication between the PC and the ASICs. The third controller allows control and monitoring of the hybrid low voltage power consumption. The low voltage regulators are mounted on the FE adapter which can be controlled via the ARC board.

4 The ARC Front End Adapter

The ARC FE adapter [12] is the second important element in the framework of the ARC test setup. This adapter card consists of two printed circuit boards (dimensions: 72mm $\times$ 72mm) stacked onto each other. The hybrid is connected to the ARC FE adapter which is directly connected to the ARC board via one 26 pin twisted pair flat cable (figure 1).

Three function groups are housed on the first printed circuit board. An I^2C level shifter which serves as a bi-directional FET shifter, three differential input and differential output buffers are used for analogue data buffering and the clock and trigger function group. The second board houses the voltage regulation circuit for the hybrid low voltage. The separation of the high power dissipating part from the FE adapter facilitates the use of the ARC system for hybrid and module thermal cycling tests. Only the level shifter and the analogue buffer need to be close to the hybrid while the high power part can be located away from the hybrid.

The hybrid power regulator is designed as a voltage tracking regulator to avoid reverse currents due to failures on a hybrid, i.e. V125 is always half of V250. Another feature of the ARC FE adapter is the capability of controlling hybrid currents and voltages on the two power lines via the I^2C interface[5)]. The voltages can be adjusted within a range of +4%/-15% compared to the nominal voltages. Safety concerning hybrid power consumption is guaranteed by an overvoltage protection and a current limiter. If one voltage increases the nominal voltage by more than 8% the hybrid voltage supply is cut off to prevent hybrid damage. The current limiter is set to 1.3 A on the V250 and to 0.9 A on the V125 power line. The values chosen were found reasonable after the experience gained with a hybrid equipped with four APVs. Hybrid voltages and the corresponding currents are read out by software and displayed on the monitor screen.

5 Additional Features of the Test Facility

One important feature is the low cost of the ARC test setup (see table 2).

[5)] The hybrids are biased with two voltages see section 7.3

Device	Price [CHF]
ARC	1100
ARC Front End Adapter	190
PCMIO interface	120

Table 2: Preliminary cost estimation of the test setup.

The concept of the ARC system allows extension to a complete functional silicon detector module test setup. Such a module test setup has to provide a high voltage power supply (up to 600 V) and a current measurement device with good resolution. The integration of a HV power supply into the setup is under development. For tests concerning the signal performance of a silicon detector the ARC board supports an external trigger capability (see the external trigger connector on figure 2). So the system can be triggered by any kind of NIM pulse generated by LED pulsing generators or scintillators, for example.

Another important feature concerns the FE adapter which can be used as a standalone tool for tests which do not require the readout of APV analogue data. Because of its own I^2C control link, this adapter can be connected directly to a serial port (RS 232) of a PC via a specifically designed small interface. This interface transfers the I^2C protocol to the serial port. With such a compact test setup (one FE adapter for one hybrid, one +5 V power supply, the small interface and one standard PC) all checks concerning slow control and low voltage control can be done easily. Because all basic functionality tests of the FE hybrid and the ASICs are feasible the ARC is also an ideal tool for fast tests in industry.

6 The APV Readout Controller Software ARCS

A specific graphical user interface for data acquisition and first data analysis purposes is evolving in Aachen. This software application is called APV Readout Controller Software (ARCS) and was developed using LabVIEW 6i [13]. LabVIEW is a widespread graphical programming tool that enables the design of userfriendly application environments. Additionally the connection of a LabVIEW application to a database is well supported. The direct communication between ARC and the application is based on dynamic link libraries or shared libraries written in C/C++ language embedded in the LabVIEW code. The use of C code provides the flexibility of the software in case of implementations of automatic test procedures. The LabVIEW programming environment supports a stable application performance under WINDOWS 9X and Linux platforms. Although LabVIEW is a licensed software package, a so called real-time player distributed by National Instruments is available on the world wide web [14] without license fees[6)]. The installation of this free real-time player is sufficient to run ARCS and thus avoiding expensive license fees.

The current status of ARCS can be divided into two main topics:

- *Monitoring* and storage of FE hybrid data: The structure of ARCS is based on the sequences needed to read out the ASICs. After a proper initialisation of the ARC board itself and the I^2C controller (including an I^2C address scan), it is possible to communicate with the chips. The writing and reading of the chip parameters finalises the so–called initialisation phase. The subsequent phase includes the monitoring of hybrid data where the display of APV frames and the hybrid currents and voltages are enabled. The online monitoring of the APV data (ordered or unordered data, raw data, pedestal corrected data) delivers first indications of the functionality of the tested FE electronics. Additionally raw data or pedestals, rms noise and gain can be written to disc or to the database enabling detailed offline analysis.

- *Automated Fast Tests* intended for industry purposes: Based on experiences gained with one preprototype FE hybrid (see below), a table of selectable tests is provided in ARCS. These tests will be executed automatically. A passed test is indicated by a green and a failed test by a red light. All results are written into ASCII files.

A screenshot of ARCS during the monitoring phase is shown in figure 3. The index card register on the left side enables the control of all ASICs, data storage and manipulation of the data which is displayed in the big box on the right side of the screenshot. Currently chosen is the APV Display card on which the position of the APV chips on the FE hybrid is shown and APV data is related to the big box by using different colors. The frames of four

[6)] This concerns Win 9x platforms, the Linux real-time player is not available without a licence.

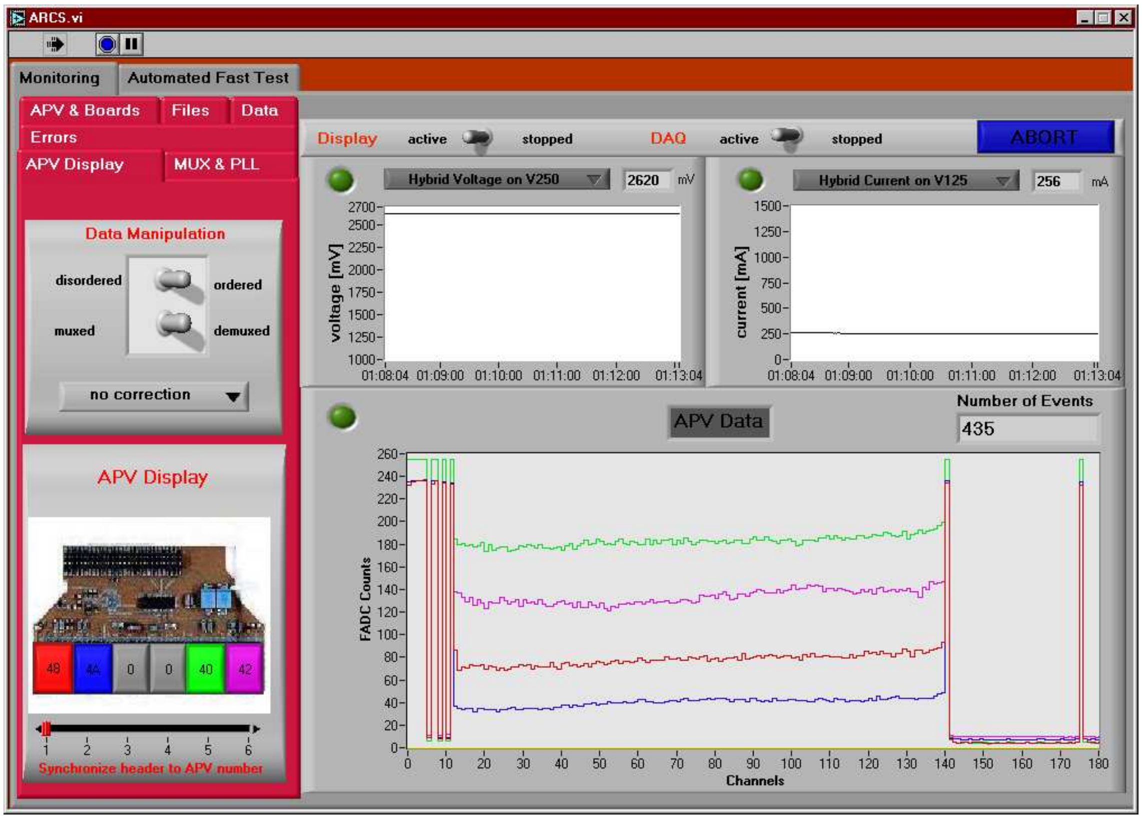

Figure 3: Example of a screenshot of the APV Readout Controller Software (see text for more details).

APVs can be seen starting with the digital header followed by the analogue data of the 128 APV channels and two tick marks at the end. On the top right side the voltages and currents are displayed. Detailed information about the operation of ARCS can be found in [15].

7 Results

In this section results of hybrid tests based on measurements with one so called preprototype FE hybrid equipped with four APV25 S1 and one PLL/MUX chip[7)] some feasible hybrid tests are presented. The hybrid is tested with a single board ARC setup described in section 2.2 and using the ARCS. If not mentioned explicitly, default chip parameter settings are chosen which are listed in [3, 4, 5].

7.1 Testing of the I^{2}C Communication

To avoid wrong diagnosis, the very first step in the chain of hybrid tests should verify the test hardware itself. Therefore the communication between the ARC board and the PC has to be checked to guarantee an operational test setup.

Afterwards hybrid functionality tests can start with a check of the I^{2}C communication. This includes an I^{2}C address scan which is based on the response of all involved chips. In this context the acknowledgement of a chip is sensitive to the logical low level. The acceptance of the logical low level itself depends on the hybrid voltage supply. Figure 4 shows the number of I^{2}C addresses found as a function of the voltage supplied to the hybrid. The I^{2}C address scan was done many times for a selected voltage explaining the different numbers of found I^{2}C addresses in some regions of the abscissa. The measurement is based on a logical low level of 300 mV.

On the tested hybrid all I^{2}C lines respond at the nominal supply voltage of 2.5 V if the logical low level is lowered to 100 mV. This solution has been adopted for the CCU module designed at CERN. The procedure described in this paragraph represents a simple test method for the logical levels of the tested hybrid.

[7)] The DCU chip was not available during the production of this preprototype FE hybrid.

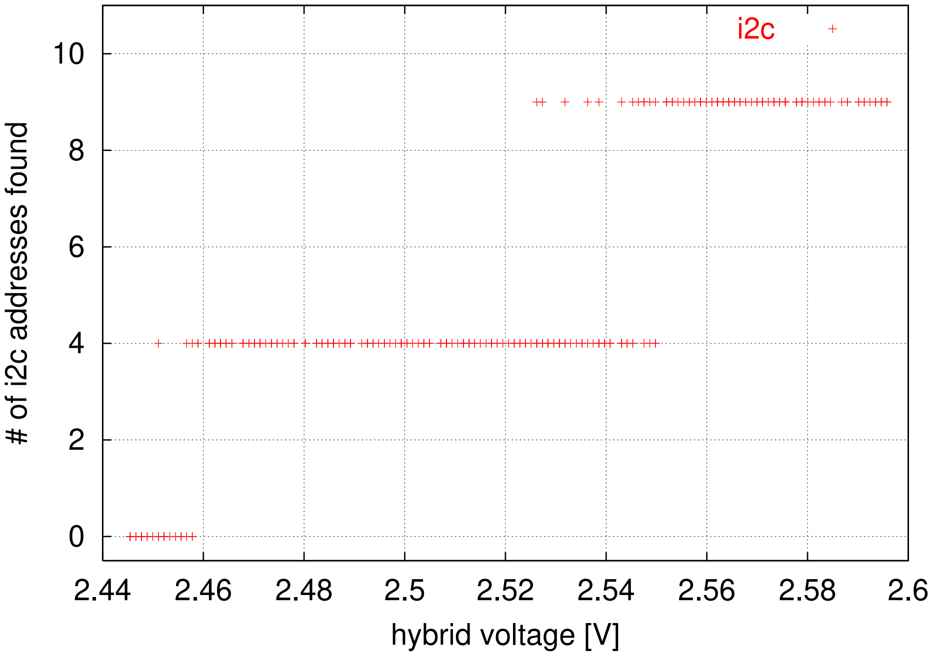

Figure 4: Acknowledgement of the hybrid ASICs as a function of the hybrid power within the ranges of 2.44 V to 2.6 V (with a resolution of 4 mV).

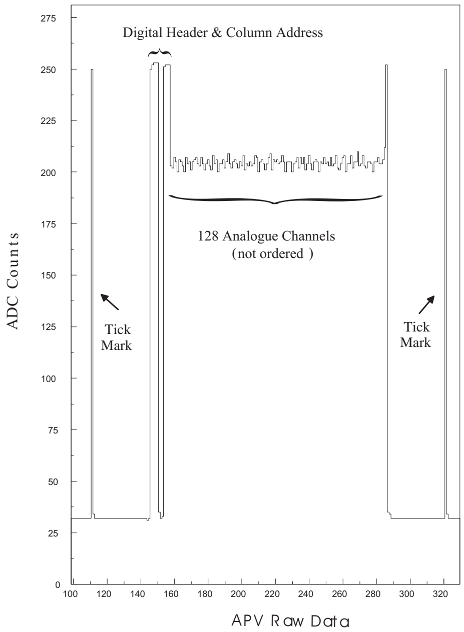

Figure 5: APV raw data frame including header, column address, analogue data and tick marks.

The acknowledgement of all chips is mandatory for a propper communication between a hybrid and the readout electronics. Since I^2C communication test procedures take only a few seconds(<30s), they should be a part of the hybrid tests done in industry.

7.2 Testing of ASIC Characteristics

In contrast to the basic tests described above, testing the ASIC characteristics requires more detailed data analysis. Most of these tests will also be done directly after the chip production.

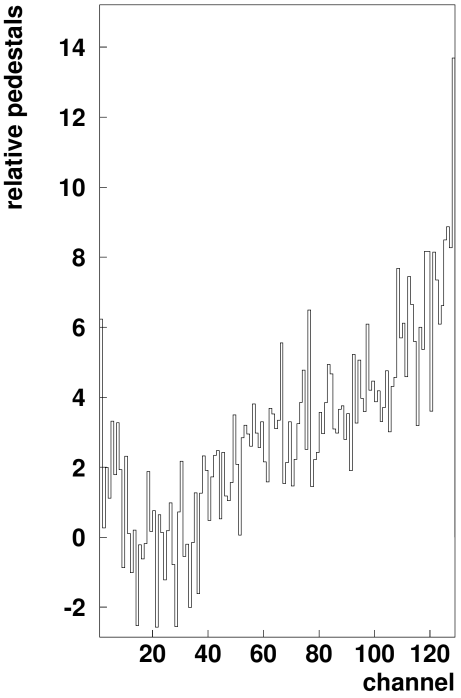

Figure 6: Average pedestals relative to the mean baseline for each of the 128 channels of the same APV used in figure 7.

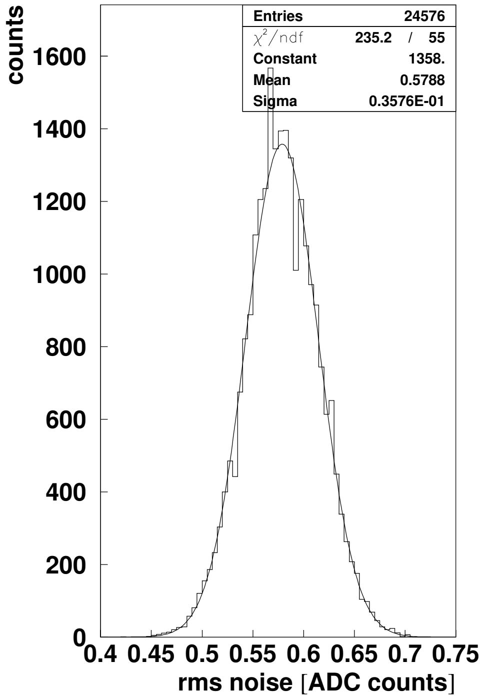

Figure 7: Rms noise of a scanned APV25 S1 plotted in units of ADC counts (one ADC count corresponds to $\approx$ 400 electrons).

7.2.1 The APV Chips

The so-called APV frame gives obvious indication of possible failures in the APV output data. As described in [3] the data output format is made up of four parts: a digital header, a digital column address, an error bit and an analogue data set (see figure 5). The error bit flags the appearance of a FIFO or latency error (the bit is switched from logical 1 to 0 if an error occurs). Additionally the column addresses of all APV chips placed on the same hybrid should always be identical. Deviations of the individual column addresses and all flagged errors have to be detected by the data acquisition software during the test procedure.

Another important evaluation of the hybrid functionality is derived from pedestal, noise and gain data. Therefore analysis algorithms are defined calculating these values from the raw APV data. Figures 8 and 9 show the rms noise distribution of each channel and each column and the pedestals calculated online relative to the average data baseline. If the data within each channel do not change much, the pedestals can be plotted averaged over all 192 columns without significant loss of information (figure 6). Figure 7 stresses the low level of noise on the examined chip. These results are based on the APV operation in peak mode and one activated MUX resistor.

7.2.2 The PLL and MUX Chip

The MUX chip multiplexes the output of two APV25 chips onto a single channel. The functionality of this chip can be tested by examining the two resulting APV frames after the demultiplexing process. Switching all termination resistors of the MUX sequentially on and off gives also an indication of a correct operation as the height of the digital 1 (in ADC counts) in the APV header is sensitive to the number of switched resistors.

Operating the PLL chip in normal mode initialises an auto calibration circuit which causes the PLL to work with reliable default settings. This initialisation can be done by sending a reset sequence. A successful completion of the calibration cycle is flagged by one status register bit [4]. Several auto calibration cycles have to be done to prove the correct read and write access of the PLL chip.

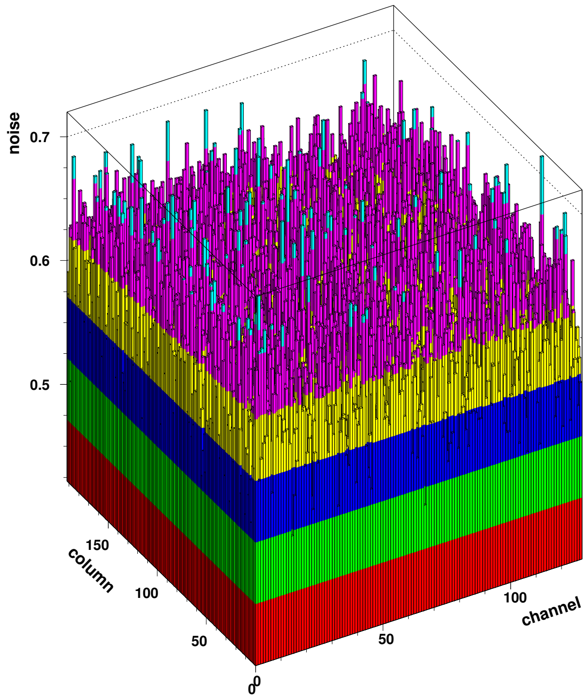

Figure 8: Rms noise matrix of an APV25 S1 chip (peak mode). The calculation of noise can be found in [15].

7.2.3 The DCU Chip

The test system presented here is designed to provide full communication with the four I^2C registers of the DCU, but as no DCU chip was available on the existing preprototype FE Hybrid, no tests of this chip could be performed. Therefore the DCU control and readout is not yet part of ARCS.

7.3 The Hybrid Power Consumption

The third main point within the chain of the hybrid test procedure is represented by the control and measurement of the hybrid power consumption. As the hybrid is biased at 1.25 V (V125 line) and 2.5 V (V250 line), there are two current values that have to be monitored. Figure 10 shows an example of hybrid current measurements as a function of the input voltage on line V250. To prevent the ASICs from being over-biased, the FE adapter is equipped with over-voltage and over-current protection (see section 4).

The capability of measuring the hybrid currents leads to a very important aspect of quality tests: to guarantee a reasonable power consumption of each hybrid during detector operation it is mandatory to spot dependencies between currents and register settings on the probed hybrid. As an example figure 11 demonstrates the strong current dependence on the setting of the IPSP APV register. Therefore a functionality test of a FE hybrid should include at least two current measurements: with default register settings and with the worst combination of register settings (which still has to be defined).

8 Possible Hybrid Test Scenario

Two test scenarios for FE Hybrids are listed in tables 3 and 4 concerning fast industry and thorough tests. These proposals are based on the experience gained during the studies with the single preprototype FE hybrid that is available in Aachen.

9 Conclusions

The described FE hybrid test facility ARC represents a compact, low cost package (about 1600 CHF including one ARC board, two ARC FE adapter and one ISA interface) which provides full operation and test of FE hybrids.

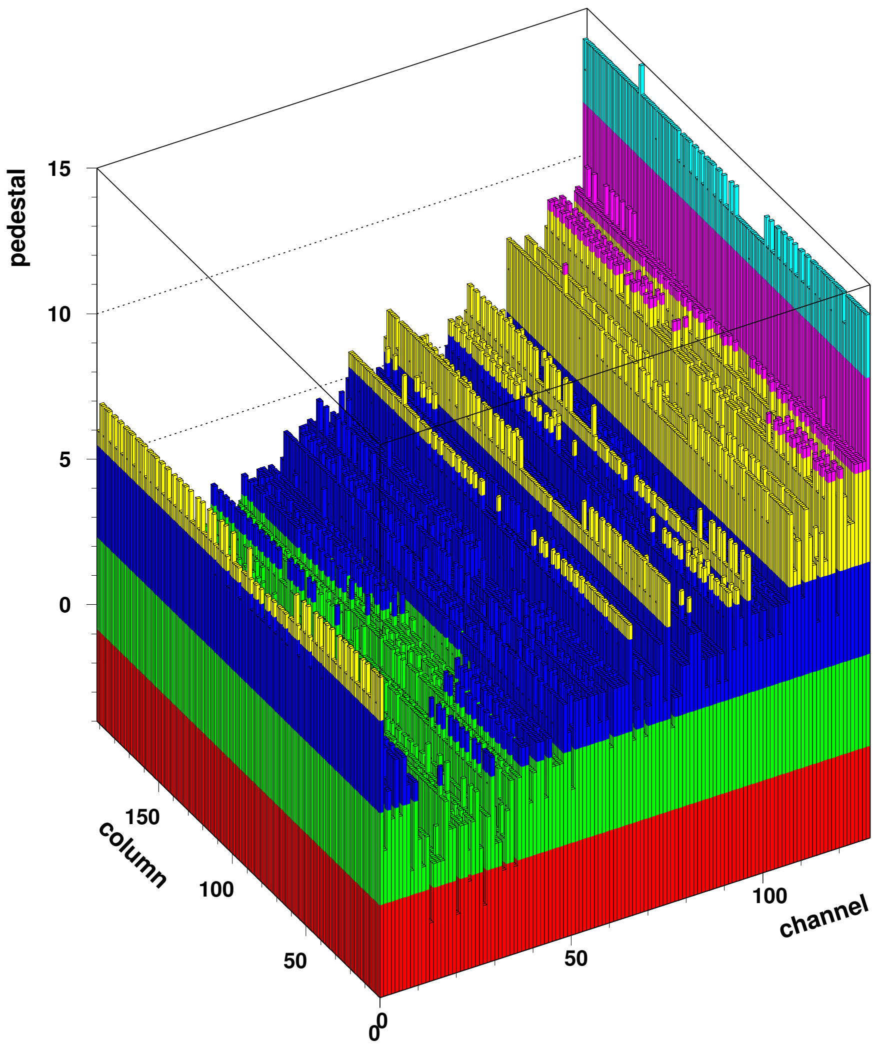

Figure 9: Relative pedestal matrix of an APV25 S1 chip operating in peak mode. The calculation of pedestals can be found in [15].

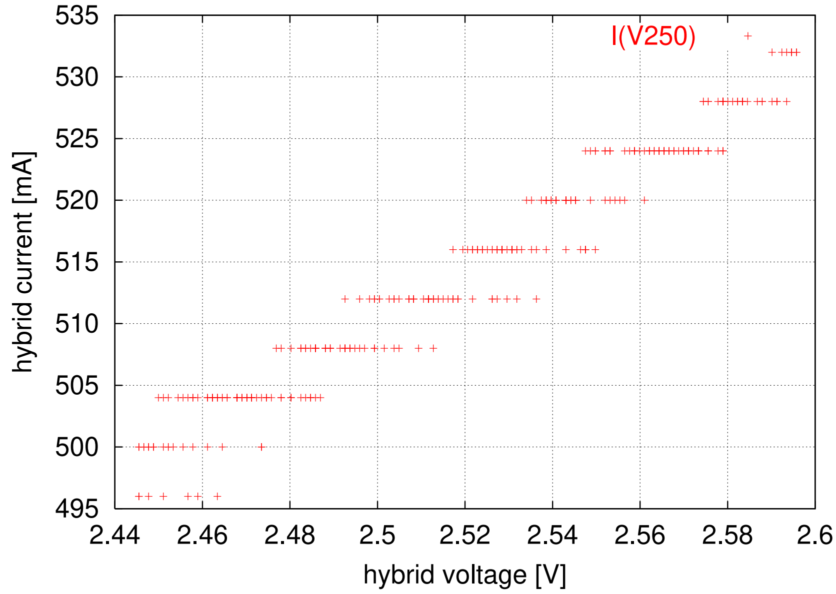

Figure 10: Dependence of the hybrid current from the hybrid input voltage on the V250 line measured simultaneously with the I^{2}C response tests (figure 4). The corresponding resolutions are 4 mV resp. 4 mA and the voltage values have been changed randomly within the shown range.

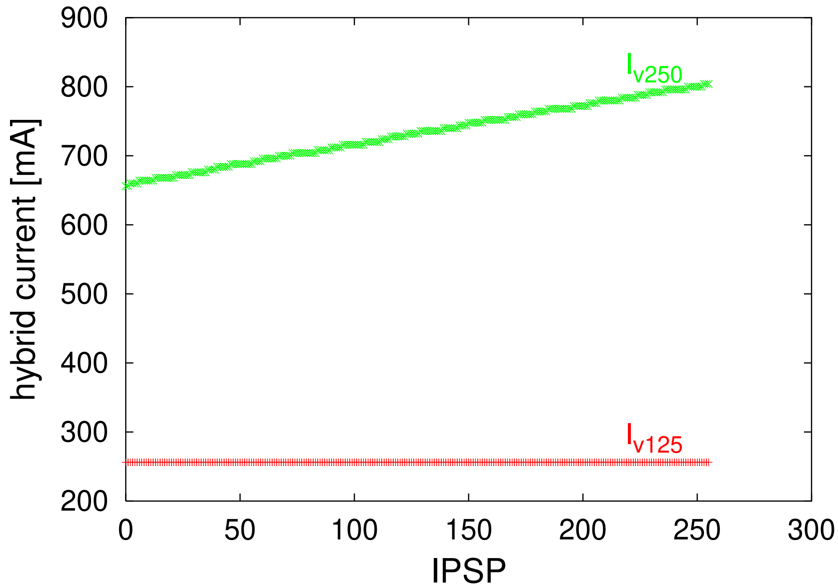

Figure 11: The hybrid currents of the lines V125 and V250 are plotted as a function of APV25 IPSP values in the range of 0 and 255. All other chip registers are set to default values.

Type of Test	Comments	Duration
1) ARC hardware accessibility	guarantee an operational system check starting conditions without any register setting	the total duration of these test procedures is about 20 to 30 sec, depending on the kind of interface and the settings
2) FE Hybrid low voltage and current measurements on V125 and V250		
3) IC address scan 4) Read and write cycles of ASIC register settings	ensure the accessibility of the ASICs check the response	
5) Count of APV header and column errors	check APV synchronization, timing and clock distribution	

Table 3: A possible test scenario for fully equipped FE hybrids to be performed in industry (in recommended order). These tests can be performed within an automated test procedure in version 2.0 of ARCS.

Type of Test	Comments	Duration
1) see table 3	these are mandatory tests !	4min
2) *APV25*: calculate pedestal matrix, rms noise matrix in peak and deconvolution mode calculate gain in calibration mode	calculations in [15] prove APV performance	
3) *PLL*: initialise autocalibration cycles run in test mode: shift clock and phases		
4) *MUX*: check output gains	check resistor operations	
5) *DCU*	chip is not implemented now	
6) measure hybrid currents on V125 and V250 in dependence of register settings (default and worst case)		2min

Table 4: A possible test scenario for FE hybrids which is intended for thorough functionality tests in the institutes (currently there is no automated test procedure implemented in ARCS, but all tests can be done manually). Most of these tests are too time consuming to be done in industry.

One package is suited to serve two hybrids simultaneously (*single board setup*), but it can also be extended to a *multi board setup* by daisy chaining of up to twenty ARC boards inserted into a standard 19" crate. So this test facility is suited on the one hand for individual, thorough tests and on the other hand for mass tests during the hybrid production. That means the ARC is a tool for first diagnostics in the industry and for thorough test in the participating institutes.

The APV Readout Controller Software (ARCS) is specially designed as graphical user interface for the ARC setup. ARCS is based on LabVIEW which is a widespread, complex graphical programming environment for laboratory issues (userfriendly applications, easy database connection, reasonable handling of a huge amount of data, easy implementation of automatic test procedures etc.). The ARCS application runs with the LabVIEW real-time player without license fees on standard Win 9x platforms.

The functionality of the complete ARC test setup was proven by measurements performed with one preprototype FE hybrid (equipped with 4 APV25 S1) at Aachen and one preprototype FE hybrid (equipped with 6 APV25 S1) at CERN. The experience concerning the functionality of FE hybrids gained in Aachen leads to proposed test scenarios for FE hybrids (tables 3 and 4). Additionally the concept of the ARC setup allows the extension to a silicon module test facility.

References

[1] Homepage Aachen: AMS Group, *"http://www.physik.rwth-aachen.de/group/IIIphys/Electronics/ams.html"*

[2] Homepage Aachen: CMS Group, *"http://www.physik.rwth-aachen.de/group/IIIphys/CMS/tracker/index.html"*

[3] Jones, *"APV25-S1 User Guide"*, Version 1.1, April 14th, 2000

[4] Placidi, Marchioro, Moreira, *"CMS Tracker PLL Reference Manual"*, Version 2.0, July 2000, CERN

[5] Murray, *"APVMUX User Guide"*, Version 1.0, May 9th, 2000

[6] Magazzu, Marchioro, Moreira, *"Detector Control Unit (DCU) for the CMS Tracker"*, February 2000

[7] Goerlach, Berst, *"Market Survey: Description and Technical Specifications of the CMS Tracker Front End Hybrids"*, Version 2.3, March 14th, 2001

[8] Beissel, Camps, *"SRDPC and SRD104-MIO - ISA Bus Extender Module for Memory- or IO-Access"*, Version 1.2, August 28th, 2000, III. Physikalisches Institut B, RWTH Aachen

[9] Commichau, Hangarter, *"EPPISA and SRDEPPC, Enhanced Parallel Port to ISA or SRDPC Converter"*, Version 1.2, March 14th, 2000, III. Physikalisches Institut B, RWTH Aachen

[10] Axer, Beissel, Camps, Commichau, Hangarter, *"ARC - A Super Simple To Use APV Readout Controller"*, Version 1.0, May 9th, 2000, III. Physikalisches Institut B, RWTH Aachen

[11] Philips Semiconductors, *"Data Sheet: PCF8584 I^2C-bus controller"*, August 29th, 1995

[12] Beissel, *"ARC FE"*, Version 1.0, May 29th, 2001, III. Physikalisches Institut B, RWTH Aachen

[13] National Instruments, *"LabVIEW–Professional Development System for Windows, Linux"*, Version 6.0, 2000

[14] National Instruments, *"http://www.ni.com"*, (follow links: *Products* and *LabVIEW Real-Time*)

[15] Axer, Beissel, Camps, Franke, Ilgin, Niehusmann, Nowack, Poettgens, *"ARCS - APV Readout Controller Software, A Graphical User Interface for Hybrid and Module Testing"*, Version 1.1, April, 2001, III. Physikalisches Institut B, RWTH Aachen