DCU2 User Guide

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IMPORTANT NOTICE

I2C register addressing and functions
have changed significantly since version 1.1

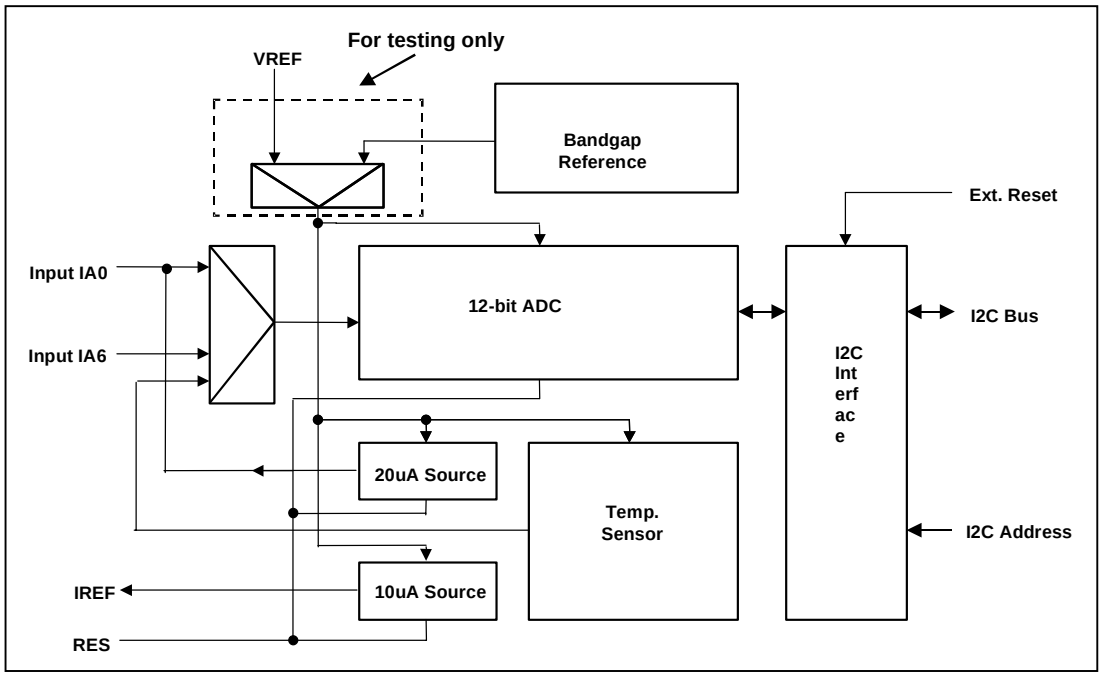
Introduction

This document is a simplified user manual for the first version of the integrated Detector Control Unit, a special ASIC to be used mainly in the CMS central tracker for the monitoring of some embedded parameters like supply voltage and currents on the front-end read-out modules.

This version of the ASIC is the final one, as from the specifications required by CMS

DCU Architecture

The architecture of the DCU2 is shown in Fig.1.



The DCU2 contains the following main blocks:

- a serial interface based on the standard I2C protocol
- a band-gap voltage reference
- an analogue multiplexer

- a 10uA constant current source
- a 12-bit ADC
- One node controller (the CCU control itself is seen as a special channel capable for instance to report the status of the other CCU channels)
- an on-chip temperature sensor
- a 20uA constant current source is available on one of the voltage measurement input pins.

The access to the internal registers of the DCU is available though an I2C interface. The user can select one of the ADC input channels, start an ADC acquisition and read the ADC output simply by accessing different I2C registers.

A band-gap voltage reference gives to the ADC a stable reference voltage. An external voltage Vref can be applied to the DCU instead of the one generated from the band-gap for test purposes only. The DCU provides one 10 uA and one 20 uA current sources that can be used to drive external thermistors for temperature measurement.

Specifications

- Digital interface I/O: I2C Standard Protocol with 2.5 V CMOS levels
- ADC Specifications
- Input channels: 7 (only 6 available in packaged version)
- Input range: 20 mV → ~ 2.5 V in two ranges.
- Reference for voltage measurements: GND or VDD (according to the selected operating mode)
- Resolution ~ 0.5 mV
- $|INL| < 1$ LSB, $|DNL| < 1$ LSB (monotonic ADC, no missing codes)
- Transition Noise RMS < 0.5 LSB
- Max Conversion Time = 0.25 usec
- Operating temperature range: -50C -> +50C
- Power consumption: < 40mW
- Supply voltage: single VDD @ 2.5V
- Clock frequency: 40MHz
- Die size: 2x2mm

- No of pads: 27 (only 24 used in packaged version)
- Available in 24 pin LPCC package or as naked die.

DCU2 Internal Registers

Register Definitions

The DCU2 contains the following 8-bit internal registers:

- Control Register (CREG)
- Auxiliary Register (AREG)
- Test Register (TREG)
- Status & Data High Register (SHREG)
- Data Low Register (LREG)

Three registers (CREG, AREG and TREG) are R/W; the remaining two (SHREG and LREG) are read only.

The access to the 4 registers follows the I2C standard protocol. The 4 MSBs of the 7-bit I2C address are used to address the chip on an I2C bus; the remaining 3 bits are used to address the five internal registers according to the following table:

Register	I2C address <A2:A0>
CREG	000
AREG	010
TREG	100
SHREG	001
LREG	011

The full address of a register is therefore given by the concatenation of the high 4 externally settable addresses with the three internal register' address

As usual on an I2C bus, for both address and data the MSB is transmitted first.

CONTROL REGISTER (R/W)

The bit allocation of the Control Register is described below:

Bit(s)	Name	Function
7	START	"1" to start an A to D conversion
6	RESET	"1" to reset the r/w registers
5	HIRES	must be "0"
4	TSON	must be "0"
3	POLARITY	must be "1"
2:0	CHANNEL<2:0>	Selects the ADC input channel

Extended Control and Test Register (R/W)

Bit(s)	Name	Function
7	CNT_TEST	Used to test AD counter, must be written with 0
6	ADCFSM_TEST	Used to test AD control logic, must be written with 0
5	Unused	
4	BGON	Selects the bandgap reference, must be written with 1
3	FSMODE	Activates single scale mode, must be written with 0
2	DTPION	Stops AD counter on external trigger, must be written with 0
1	DTPO_SEL	Selects digital test point, must be written with 0
0	ATP_SEL	Selects analog test point, must be written with 0

This register is implemented mainly for test purposes and for normal operation must always be written with 0x10.

Auxiliary Register (R/W)

Bit(s)	Name	Function
7	AD_SET	Writes into results register, must be written with 0
6	AD_RESET	Writes into results register, must be written with 0
5	Unused	
4	Unused	
3:0	FSM_STATE	Used to test control logic of AD, must be written with 0

This register is implemented only for test purposes and must always be written with 0x00.

Status & Data High Register (R/W)

The bit allocation of the Status & Data High Register is here described:

Bit(s)	Function/internal signals
7	IDLE
6	SEU Error
5:4	UNUSED
3:0	DATA<11:8>

When IDLE is equal to "1" the DCU is in the IDLE state and a new acquisition can be started. The 4 MSBs of the result of the last ADC acquisition of the can be read in DATA.

Data Low Register (R/W)

The bit allocation of the Data Low Register is described below:

Bit(s)	Function/internal signals
7:0	DATA<7:0 >

The 8 LSBs of the result of the last ADC acquisition can be read in DATA.

DCU2 Operations

HW Reset

A hardware reset of the DCU2 R/W registers is performed forcing to "0" the RESET pin.

SW Reset

A software reset of the DCU2 r/w registers is performed when a '1' is written into the bit 6 of the Control Register CREG (CREG<6>).

Acquire

An acquisition is started when a '1' is written into the bit 0 of the Control Register CREG (CREG<7>).

The bit CREG<2:0> selects the input channel according with the following table:

CREG<2:0>	ADC input channel
000	IA0
001	IA1
010	IA2
011	IA3
100	IA4
101	IA5
110	IA6
111	Temperature channel

Read Result

When the bit 0 of the Status & Data High Register SHREG<7> contains a '1', the DCU1 is in the IDLE state and the result of the last ADC acquisition can be read:

- RES<11:8> = SHREG<3:0>
- RES<7:0> = LREG<7:0>

DCU Conversion Operations

A conversion cycle of the ADC can simply be started by setting the proper channel address in the control register and setting the start conversion bit in the same register. The start conversion bit (START) is cleared automatically at the completion of the conversion. For instance, a conversion on the input channel 3 can be started by writing a "11011001" (i.e. 0xD9) into the Control register.

DCU2 Pin Layout, Package and Pin Assignments

DCU2 Pad Assignment

The DCU2 die size is 2 x 2 mm; there are 27 normal pads with a 225um pitch and 3 extra corner pads for testing purposes only.

The pad position of the 31 pads in the die is represented in Fig.2.

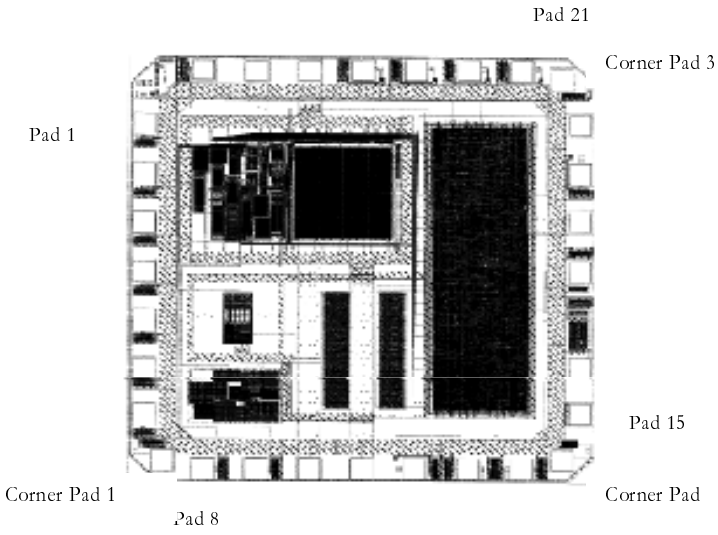


Fig.2: DCU pad position

Pad assignment

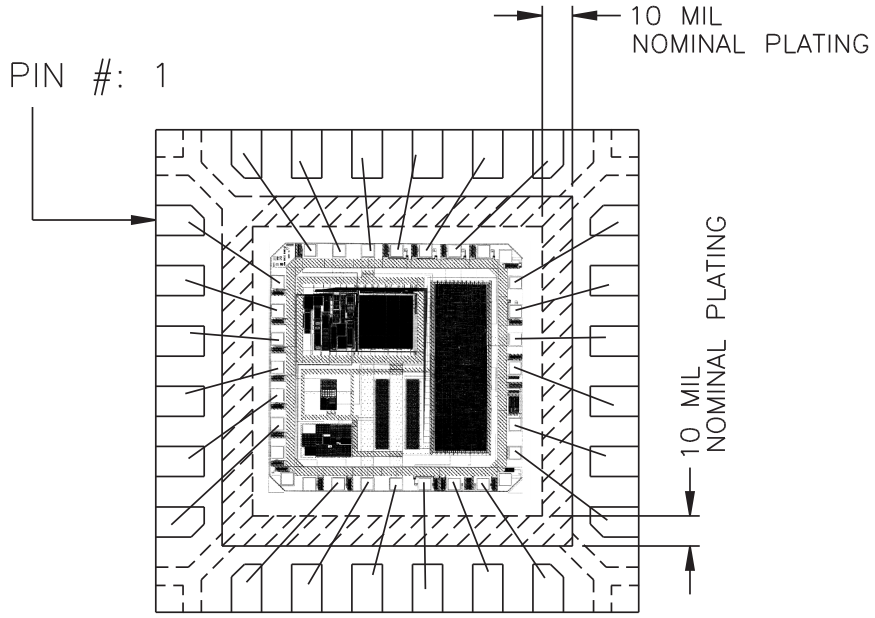
Pad assignement for DCU

Pad	Signal	Comment
1	IA0/Iout20	
2	IA1	
3	IA2	
4	IA3	
5	IA4	

6	IA5	
7	IA6	
C1	Test1	Corner Pad 1
8	Vref	
9	ExtRes	
10	GND	
11	VDD	
12	I2CA3	
13	CLK-	
14	CLK+	
C2	Test2	Corner Pad 2
15	VDD	
16	I2CSDA	
17	I2CSCL	
18	GND	
19	ResetBar	
20	GND	
C3	Test3	Corner Pad 3
21	unused	
22	I2CA6	
23	I2CA5	
24	I2CA4	
25	VDD	
26	GND	
27	Iout10	

DCU2 Packaged Version

The DCU2 bonding in the LPCC24 package is given in the figure below:



CERN - DCU

E: 1) DOTTED LINE REFER TO HALF ETCH TIE BAR POSITION
2) RING PLATING L/F; HATCHING AREA IS REPRESENTED THE DAP BONDABLE AREA.

NG DIAGRAM DRAWING NO.:		REV.:	
REVIEWED BY FOL:		DWG REVIEWED BY MOLD:	
COUNT: 24L		LEAD FRAME MATERIAL: CU, C7025	
GE DIMENSION: LPCC 4x4x0.9		LEAD FRAME THICKNESS: 8 MILS	
MER:		MAXIMUM WIRE LENGTH:	
E:		GOLD WIRE DIAMETER:	
ZE (1):		DIE ATTACH MATERIAL:	
ZE (2):		MOLD COMPOUND:	
IZE: 110x110 MILS		DRAWN BY:	DATE:
MER DOC. NO:	DATE:	REVIEWED BY:	DATE:

Pin assignment in LPCC24

Pinout for DCU in LPCC24

1	IA0/Iout20
2	IA1
3	IA2
4	IA3
5	IA4
6	IA5
7	ExtResistor
8	GND
9	VDD
10	I2CA3
11	CLK-
12	CLK+
13	VDD
14	I2CSDA
15	I2CSCL
16	GND

17 ResetBar
18 GND
19 I2CA6
20 I2CA5
21 I2CA4
22 VDD
23 GND
24 Iout10

DCU2 evaluation package

For evaluation purposes, the DCU has been packaged also in a 40-pin Dual-In-Line plastic package (DIP-40).