I^2C settings for APV operation at cold temperatures

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1. Introduction

This note gives recommendations for APV25 I^2C settings to use for a particular operating temperature, and also describes the studies that have been performed to provide these settings. It is assumed that the reader is familiar with the APV25 and has read the User Manual. A link to the User Manual and also other useful APV information can be found at:

http://www.hep.ph.ic.ac.uk/~dmray/Tracker.html

To function correctly the APV25 analogue circuitry must be correctly biased. The I^2C bias current settings (those beginning with the letter 'I') set the DC operating points of the stages in the analogue signal processing chain. The recommended values are chosen to keep the power consumption as low as possible, while still maintaining satisfactory performance. Lower values of the I^2C bias current settings correspond to lower power consumption. The performance (noise, pulse shape, linear range, ..) does not critically depend on these settings but will slowly degrade as they are reduced. Conversely small improvements in performance are possible if bias currents are raised, but at the cost of extra power consumption.

In CMS the APV bias current settings are all derived from one master internal reference current (this must be selected in the APV mode register). This master reference current is power supply, but **not** temperature, independent. For this reason the studies detailed in this note have been performed, to provide recommendations on the choice of bias current settings to maintain APV performance at different temperatures, without significant variations in power consumption.

Recommended values for CMS operation at -10° C

Table 1 lists recommended APV25 I2C bias current settings for a range of hybrid temperatures. The performance and power consumption dependence on I^2C bias register settings is such that a set of parameters can be used to cover a reasonable temperature span, at least ±5° and probably more, and therefore I suggest that the values for the -10° column in table 1 be adopted, initially, for CMS operation, to be fine-tuned as required later.

Cautionary note

While values for VPSP, ISHA and VFS **are** listed in table 1, these parameters should **still** be considered as variables. VPSP sets the analogue baseline level and should always be 'tuned' to position this appropriately, but note that the power consumption does vary with baseline position (see section 3.6). The values for the pulse shape tuning parameters ISHA and VFS listed in table 1 were found appropriate for the particular APV on the TIB module used for this test, but will not be universally applicable for other sensor types (TOB, TEC etc..). Some chip to chip variation can also be expected.

2. Experimental Set-up

The measurements on a 4 chip TIB module have been performed in a temperature controlled environmental chamber flushed with nitrogen. A diagram of the set-up is shown in figure 1. The module hybrid is in thermal contact with an aluminium plate, the other side of which is cooled by Peltier elements. The temperature is monitored using Pt100 elements on the aluminium plate and on the surface of the hybrid in the location where APVs would be mounted if it were a 6 channel module. The temperature in the chamber is also monitored. Temperatures quoted in this note are those recorded by the Pt100 sensor on the hybrid surface, and the Peltier currents are set to achieve the desired value. The environment temperature is set to the same temperature. The temperature of the hybrid surface is found, for all temperatures, to be ~ 3° higher than that on the aluminium plate. The stability of the temperature control is adequate at ~ ± 2°.

3. Results

Table 1 summarises the results of the measurements on the 4 APV25 chip TIB module. All the measurements were performed on the APV chip #5 in figure 1.

If the I2C parameters are not varied as the temperature decreases the power consumption increases. Nevertheless over a range of ~ 10° the power variations are only at the few % level so it is not necessary to re-tune parameters for temperatures varying over ranges less than this. For the measurements here the temperature has been varied in 10° steps in the range +30° down to -20°. +30° may be considered to be room temp operation but it is possible that the hybrid may reach a higher temperature if a module is operated at room temperature without any heat sink attached. At each temperature point the I^2C bias current register settings are all varied equally by a factor which achieves approximately the same overall hybrid power consumption as that at +30°. The results are shown in table 1. As the hybrid temperature is reduced the I^2C bias current parameters also reduce, although between -10° and -20° the values can be seen to be the same. This is probably because the settings were slightly over-adjusted when going between 0° and -10°, so that no further adjustment was required for -20°.

3.1. Power consumption

The currents and resulting power figures in table 1 are for the module as a whole. The power/APV can be calculated to be ~370 mW, but this figure includes an equal share of the power consumed by the APVMUX, DCU and PLL chips, which cannot be measured separately.

3.2. ISHA, VFS and VPSP

The values for ISHA and VFS in table 1 are those chosen to achieve a peak mode pulse shape close to the ideal, as can be seen in figure 2. This tuning is done “by eye”. The pulse shapes are acquired by averaging the internal calibration response for one group of 16 channels. The deconvolution response corresponding to the same tuned parameters is also shown. It was not found necessary to alter the value of VFS. **Note that the optimum choices of ISHA and VFS depend on sensor capacitance and that the values here are for one chip on a TIB module**. For other module types other values will be required, and there will likely be some module to module and chip to chip variation within module types.

For these studies the movement in the analogue baseline with temperature was found to be relatively small and so VPSP was left constant at 43. However it should be noted that APV power consumption does depend on the position of the analogue baseline (and hence VPSP) and this is discussed further in section 3.6.

3.3. Internal Calibrate (test pulse) response

Figures 3 and 4 show the internal calibration response for ICAL settings in the range 0 – 240 in steps of 40. For the same value of the ICAL register the test pulse amplitude increases with falling temperature and this relative increase is indicated in table 1. This does not correspond to an increase in chip gain in the same proportion since ICAL is derived from the master reference current.

3.4. Pulse height spectra

There is an overall increase in chip gain as temperature decreases because the gain at the 128:1 analogue MUX on the chip is set by resistors which have a temperature coefficient of 0.15%/°C. For the +30° to -20° range this should lead to a gain increase of 7.5%. The peak and deconvolution mode pulse height spectra in figures 5 and 6, obtained using a beta source, show a gain increase of ~ 7%. Going from +30° to -20°, the signal/noise ratios for the most probable signals increase from 25.7 to 29.0 and 16.6 to 17.9, for peak and deconvolution modes respectively.

3.5. What happens if the I2C settings are not tuned?

Figure 7 shows the module supply current dependences on hybrid temperature in the range -20° to +40° in the case where the I^2C settings are **not** altered from the "standard" settings (these are the values for the +30° column in table 1). I125 shows a 16 % increase as the module is cooled, which is similar to the 14% expected from simulations of the current reference circuit alone. The percentage increase of the total I250 current is smaller, but this includes contributions from the digital circuitry, which can be measured separately by switching the analogue bias to the chips off in the APV mode register. The digital supply current also has a temperature dependence, showing a 3.5 % increase over the 60° cooling range. If the digital I250 current is subtracted from the overall I250 current the resulting 'I250 analog only' current shows a 21 % increase from +40° to -20°.

3.6. Digital header amplitude and VPSP setting

The maximum and minimum levels for the digital header are also set by a current reference circuit similar to the master analogue reference and consequently the digital header amplitude also varies with temperature. Table 1 includes figures for the digital header amplitude increase, relative to that at room temperature.

For these studies VPSP was left constant for all temperatures at a value of 43. The movement of the analogue baseline with temperature was relatively small and so no adjustment was performed. It is worth noting that the module power consumption does have a dependence on the VPSP value, as can be seen in figure 8 where the VPSP dependence of the I250 current, the analogue baseline position and the total module power is shown. I250 is the total current drawn from the 2.5 Volt rail by the 4 chip module. The baseline position is the average pedestal levels of the analogue channels, relative to the full-scale digital header amplitude. The module power plot includes the power consumed from the 1.25 Volt rail, which is independent of VPSP. Lower power consumption is achieved where the baseline setting is closer to the digital baseline, but some allowance must be made for negative going displacements, such as would be produced by common mode effects. The analogue baseline level does increase slightly with reducing temperature which may account for the percentage increase in 'I250 analog only' current being higher than that for I125 in figure 2.

4. Conclusions

To avoid unnecessary extra APV power consumption when modules are operated at below room temperature in test set-ups and eventually in CMS, the I^2C parameters which govern the static power consumption in the internal analogue circuits must be chosen for operation at a particular temperature. Table 1 lists recommended values for temperatures in the range +30° to -20° in 10° steps and the values for –10 ° are those recommended for initial operation in CMS. A resolution of 10° steps between parameter changes is adequate, the sensitivity to temperature being sufficiently low.

The results presented here are for one chip on a TIB module, for which appropriate values for the ISHA, VFS and VPSP parameters were chosen. Some chip to chip and module to module variation in the optimum values for these parameters is to be expected, and significant differences between different module types are certain.

Table 1. Recommended APV25 bias parameter values (decimal) for operation at different hybrid temperatures. The values for the -10° column are those recommended for CMS operation.
* Note that values for VPSP, ISHA and VFS have been chosen for the particular APV on the TIB module studied. The optimum values for these parameters will vary from chip to chip and also depend on module type. See text for further discussion.

	Hybrid Temperature °C (± ~2°)					
	+ 30°	+ 20°	+10°	0°	**-10°**	-20°
IPRE	98	96	93	92	**85**	85
IPCASC	52	51	49	49	**45**	45
IPSF	34	34	33	32	**30**	30
ISSF	34	34	33	32	**30**	30
IPSP	55	54	53	52	**48**	48
IMUXIN	34	34	33	32	**30**	30
VFP	30	30	30	30	**30**	30
VPSP*	43*	43*	43*	43*	43*	43*
ISHA*	46*	45*	38*	32*	30*	30*
VFS*	70*	70*	70*	70*	70*	70*
relative test pulse amp. for ICAL = 40 (normalised to + 30° value)	1.00	1.04	1.08	1.12	1.17	1.21
I125 [mA/module]	220	222	222	227	214	220
I250 total [mA/module]	476	481	478	478	475	480
I250 digital [mA/module]	278	280	281	283	286	286
power [mW/module]	1465	1480	1473	1479	1455	1475
relative digital header amplitude	1.00	1.02	1.05	1.07	1.09	1.11

Figure 1. Diagram of module showing Peltier cooling and Pt100 temperature measuring points.

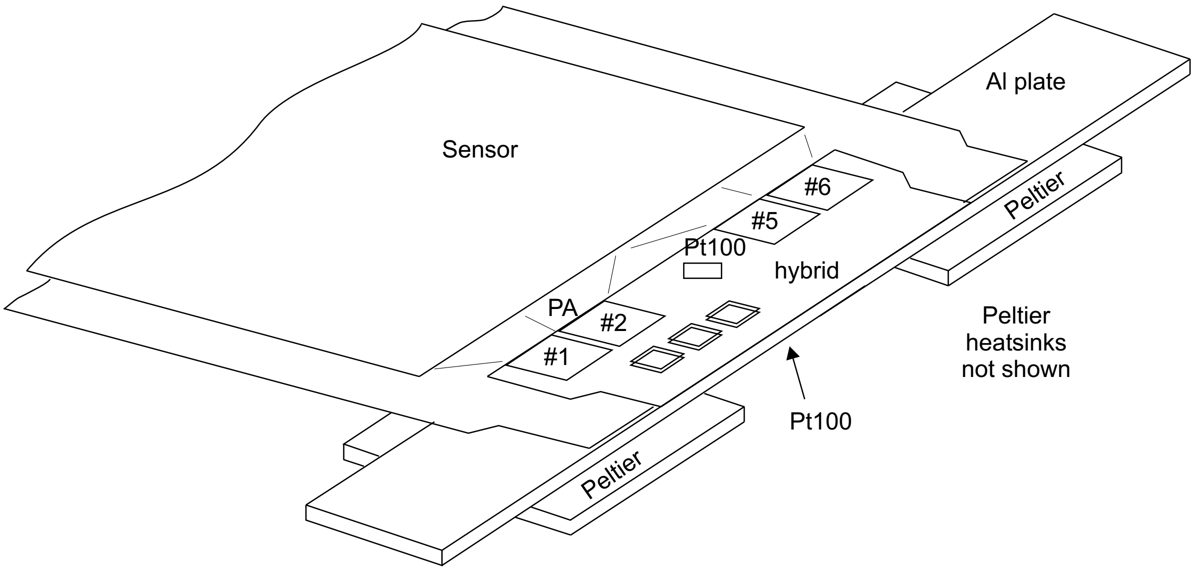

Figure 2. Peak and deconvolution mode pulse shapes obtained after tuning the ISHA parameter at different hybrid temperatures. The Pulse shapes shown are the average of 16 channels corresponding to one calibrate input. ICAL = 40, VFS = 70 in all cases. Measured peak mode pulse shape is shown in red, ideal 50 ns CR-RC pulse shape in green, deconvolution mode pulse shape in blue.

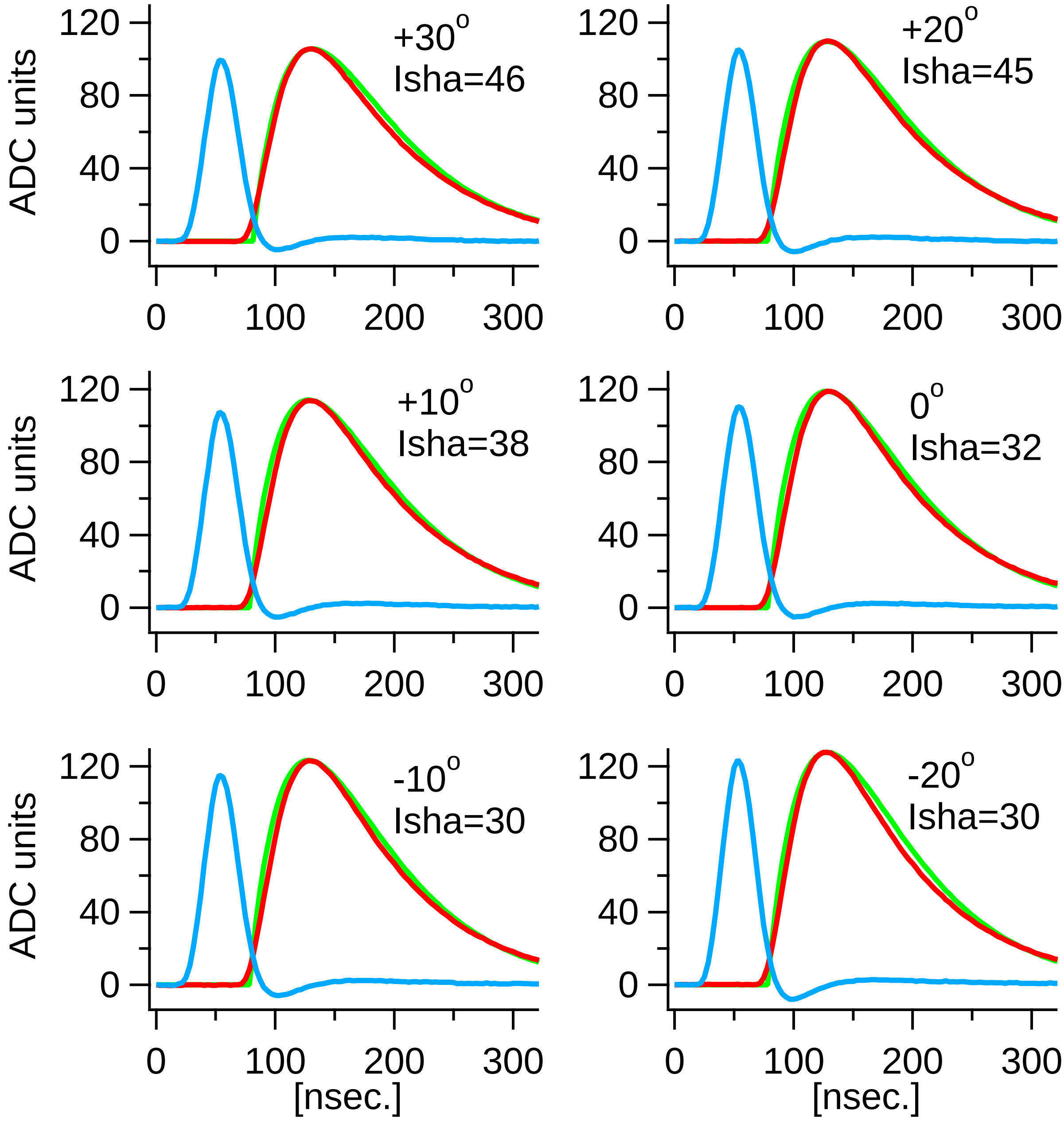

Figure 3. Peak mode pulse shapes obtained after tuning the ISHA parameter at different hybrid temperatures. The Pulse shapes shown are the average of 16 channels corresponding to one calibrate input. ICAL = 40 – 240 in steps of 40, VFS = 70 in all cases.

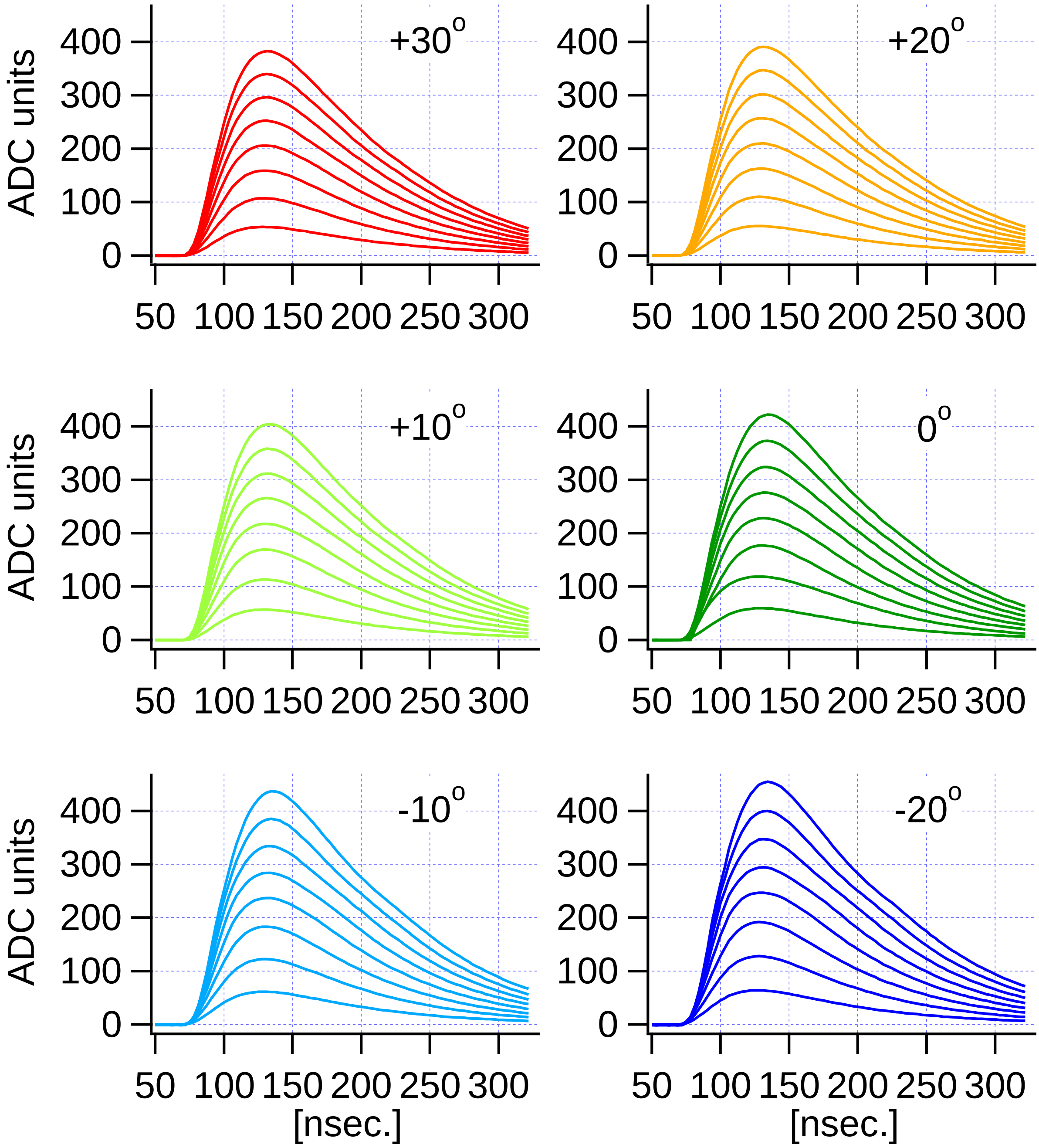

Figure 4. Deconvolution mode pulse shapes obtained after tuning the ISHA parameter at different hybrid temperatures. The pulse shapes shown are the average of 16 channels corresponding to one calibrate input. ICAL = 40 – 240 in steps of 40, VFS = 70 in all cases.

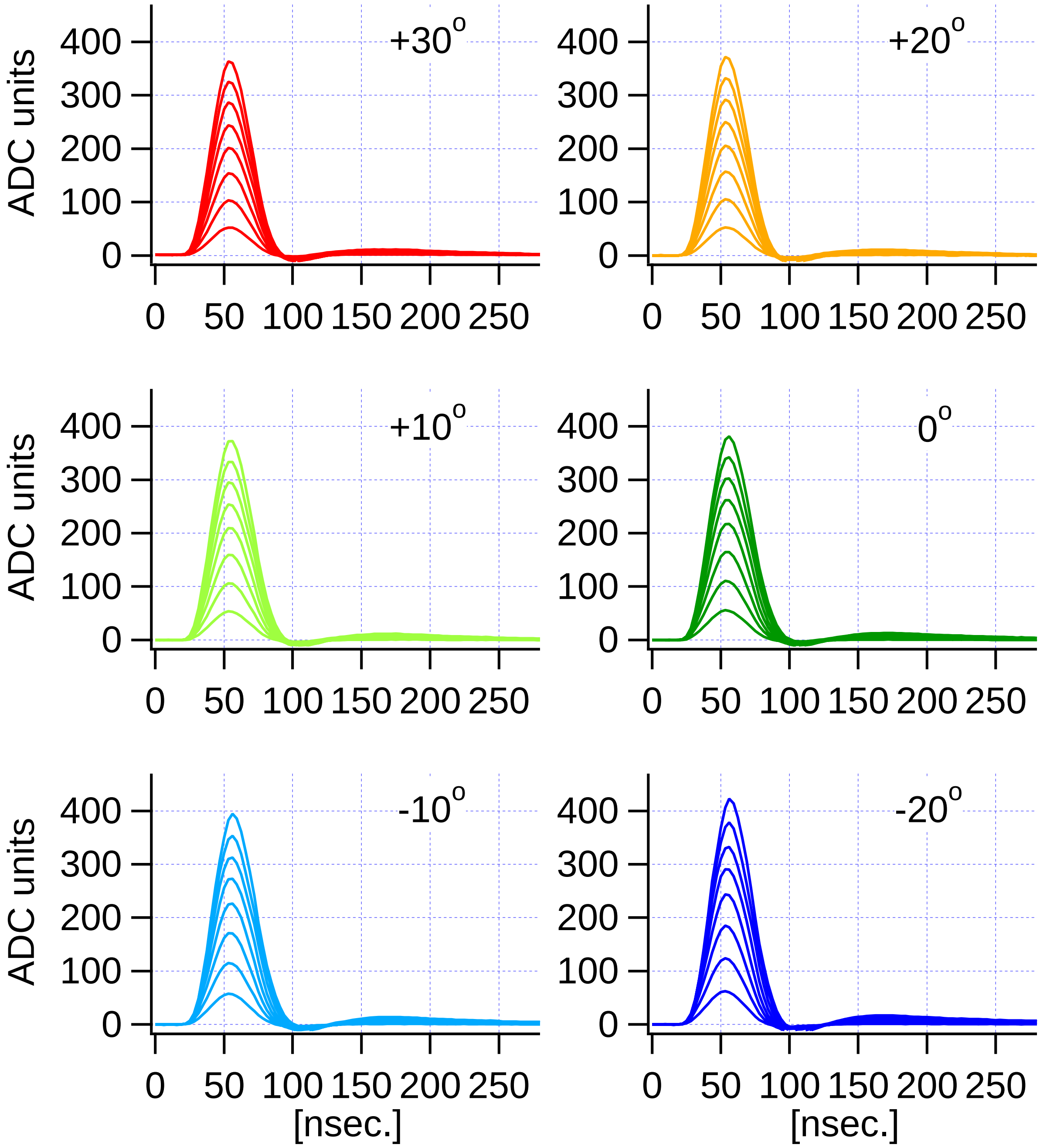

Figure 5. Peak mode beta source pulse height spectra for different module temperatures. Strip signal included if neighbouring strip signals < 3 x noise. Sensor HT = 250 V.

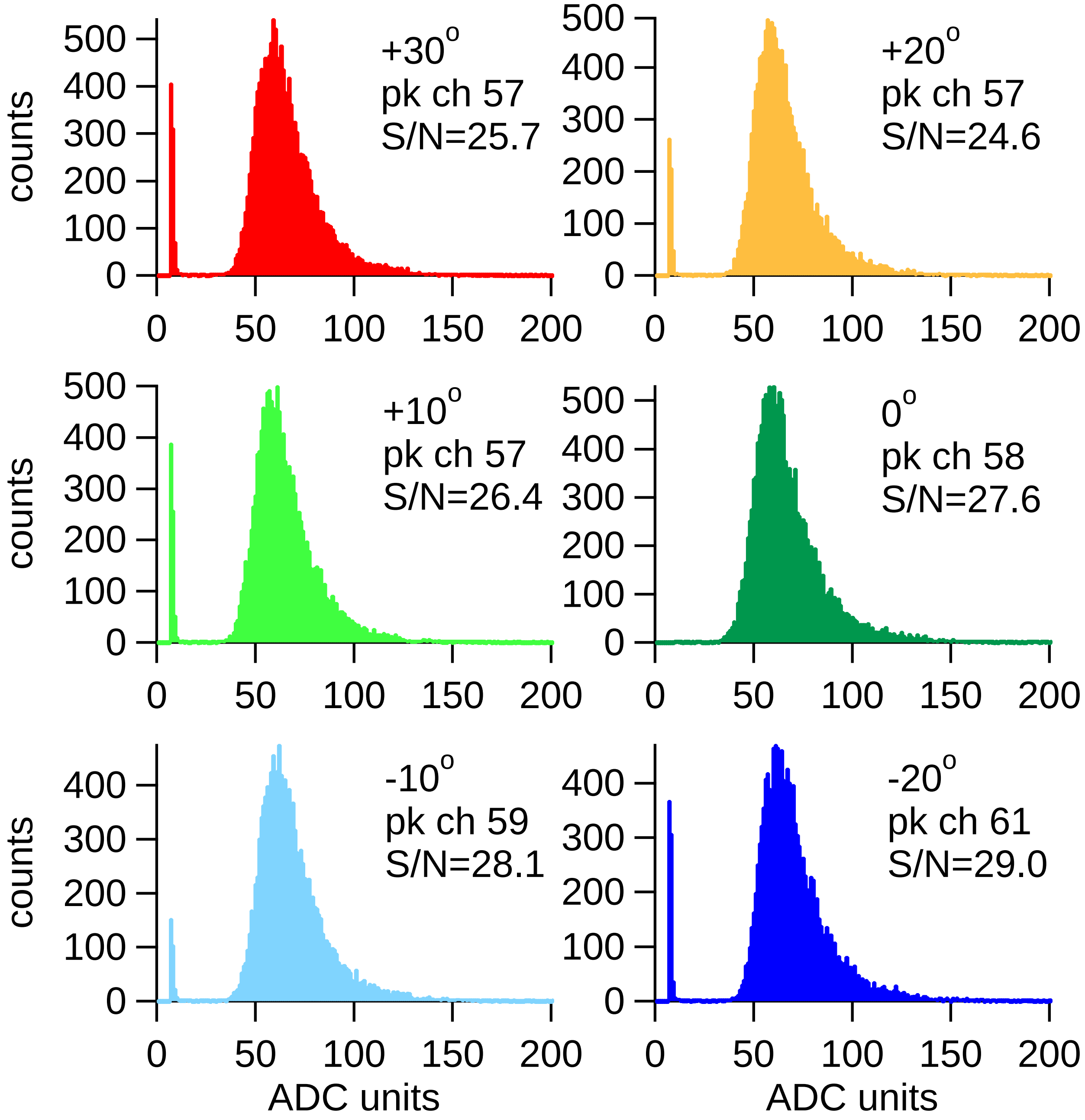

Figure 6. Deconvolution mode beta source pulse height spectra for different module temperatures. Strip signal included if neighbouring strip signals < 3 x noise. Sensor HT = 250 V.

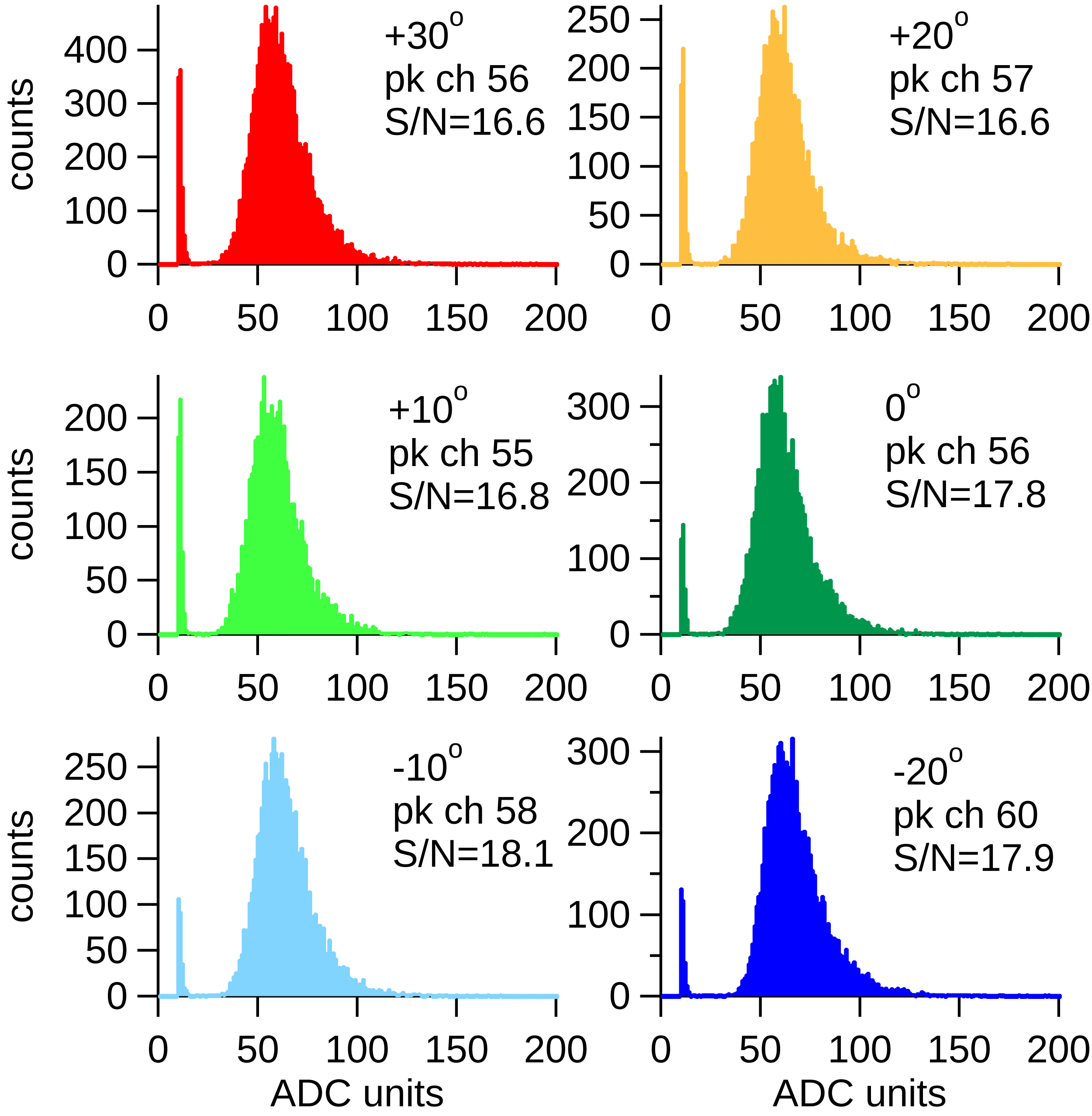

Figure 7. Temperature dependence of module supply currents if I^2C parameters are fixed at room temperature values. I125 and I250 are the total module supply currents flowing in the +1.25 and +2.5 Volt supply lines. I250 digital only is the I250 current when the APV analogue bias is switched OFF in the mode registers. I250 analog only is then I250 digital only subtracted from I250 total.

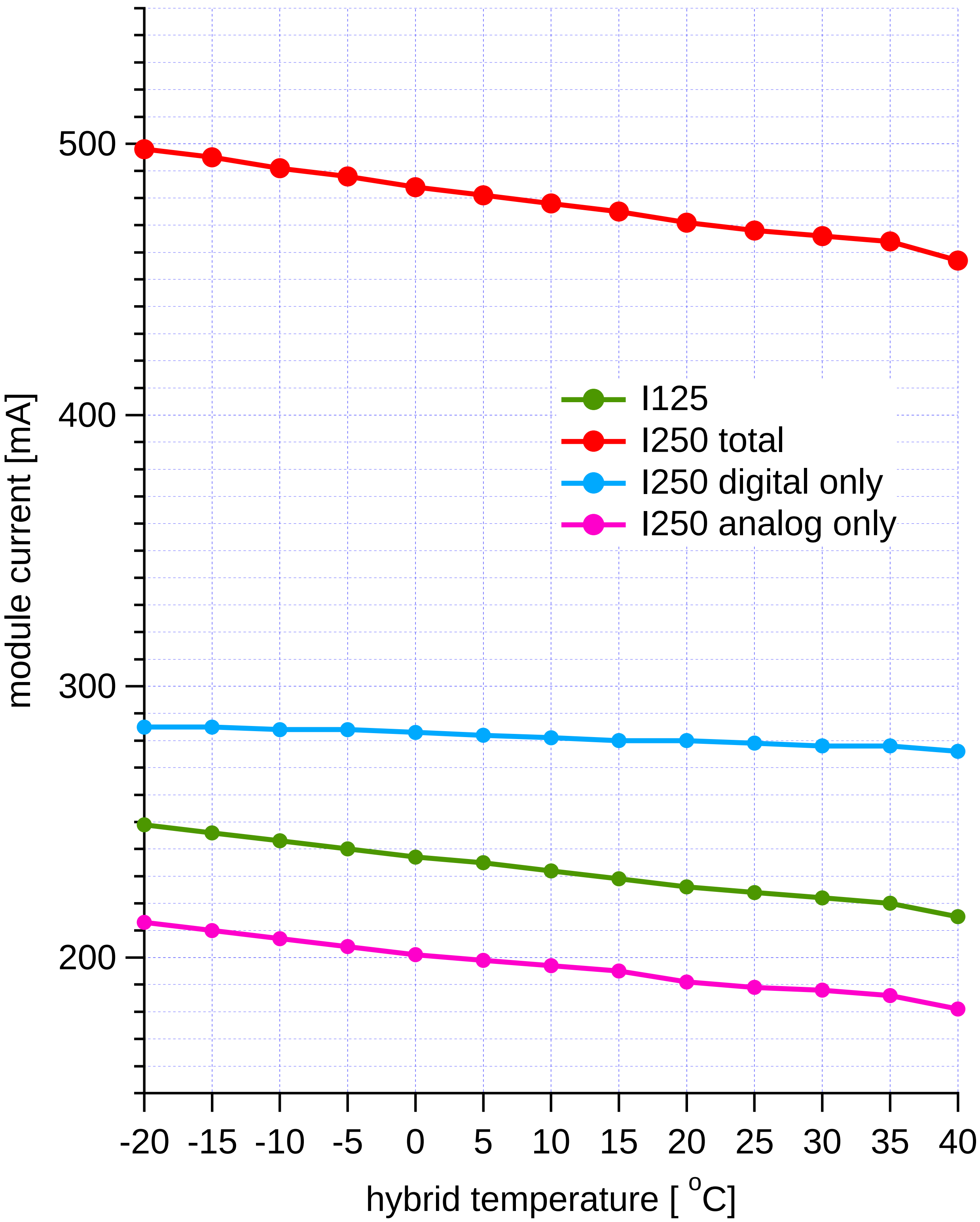

Figure 8. VPSP dependence of I250 current, analogue baseline position and total module power measured at + 30°. The analogue baseline position is normalised to the digital header amplitude (e.g. value of 0 means average channel pedestal at digital header '0' level, value of 1 means average channel pedestals level with maximum digital header amplitude). Total module power includes I125 power.