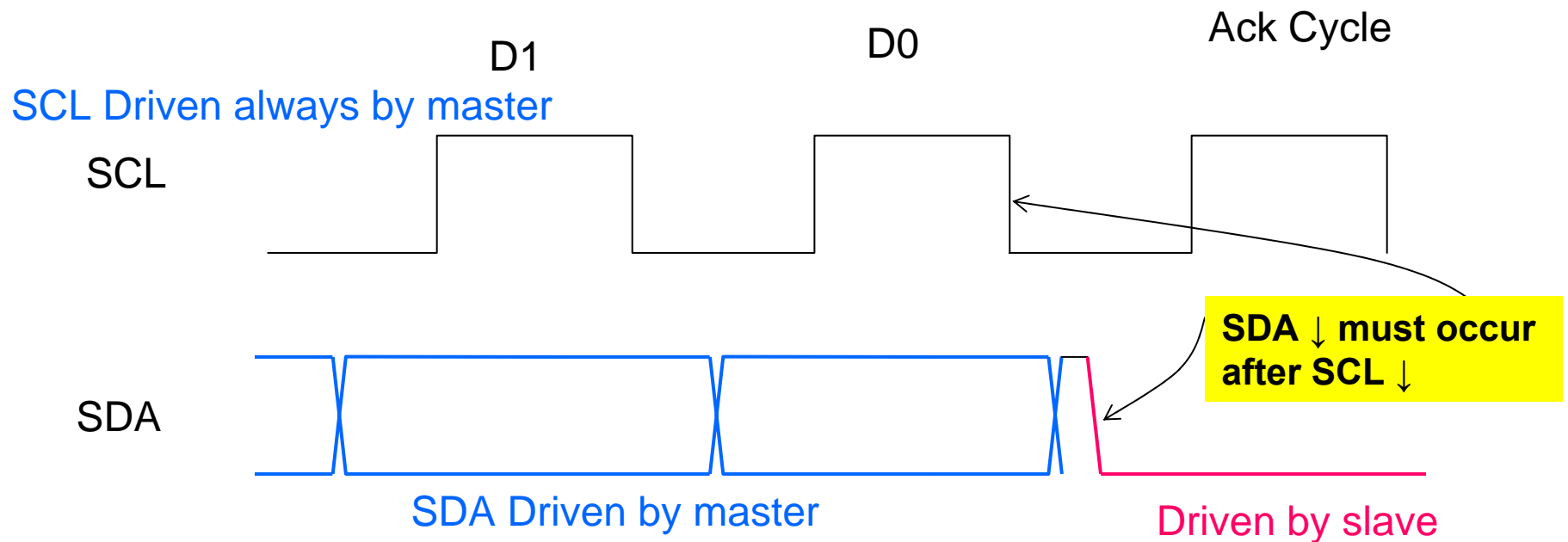


V jg! I tgc v! K 4 E ! O { wgt {
C ev! 4

V j g! hcev

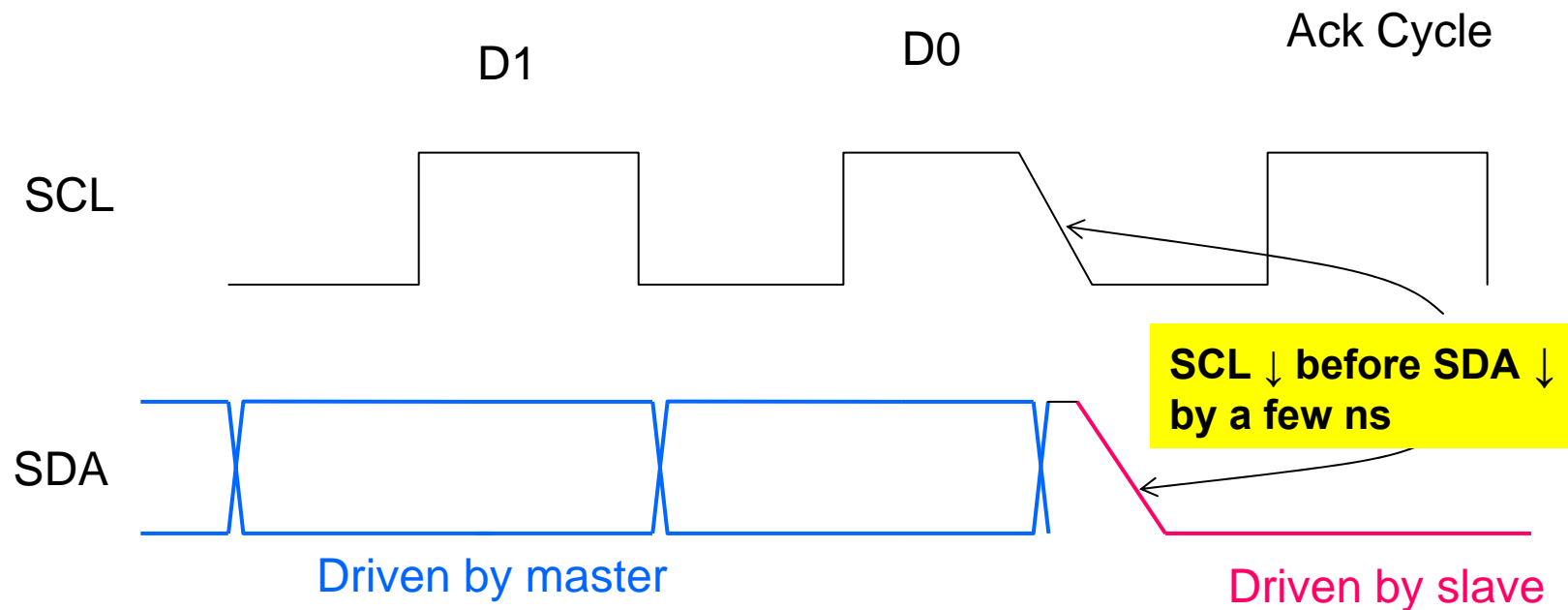
- Occasionally, when accessing sequentially components on the I2C bus (LLD, DCU etc.), the APVs are found not to respond correctly to I2C commands, actually they are stuck
 - This can data pattern dependent (as the last bit of the data sequence is the one most often misinterpreted)
- The lock-up can only be cleared by Resetting the APV

The theoretical waveforms

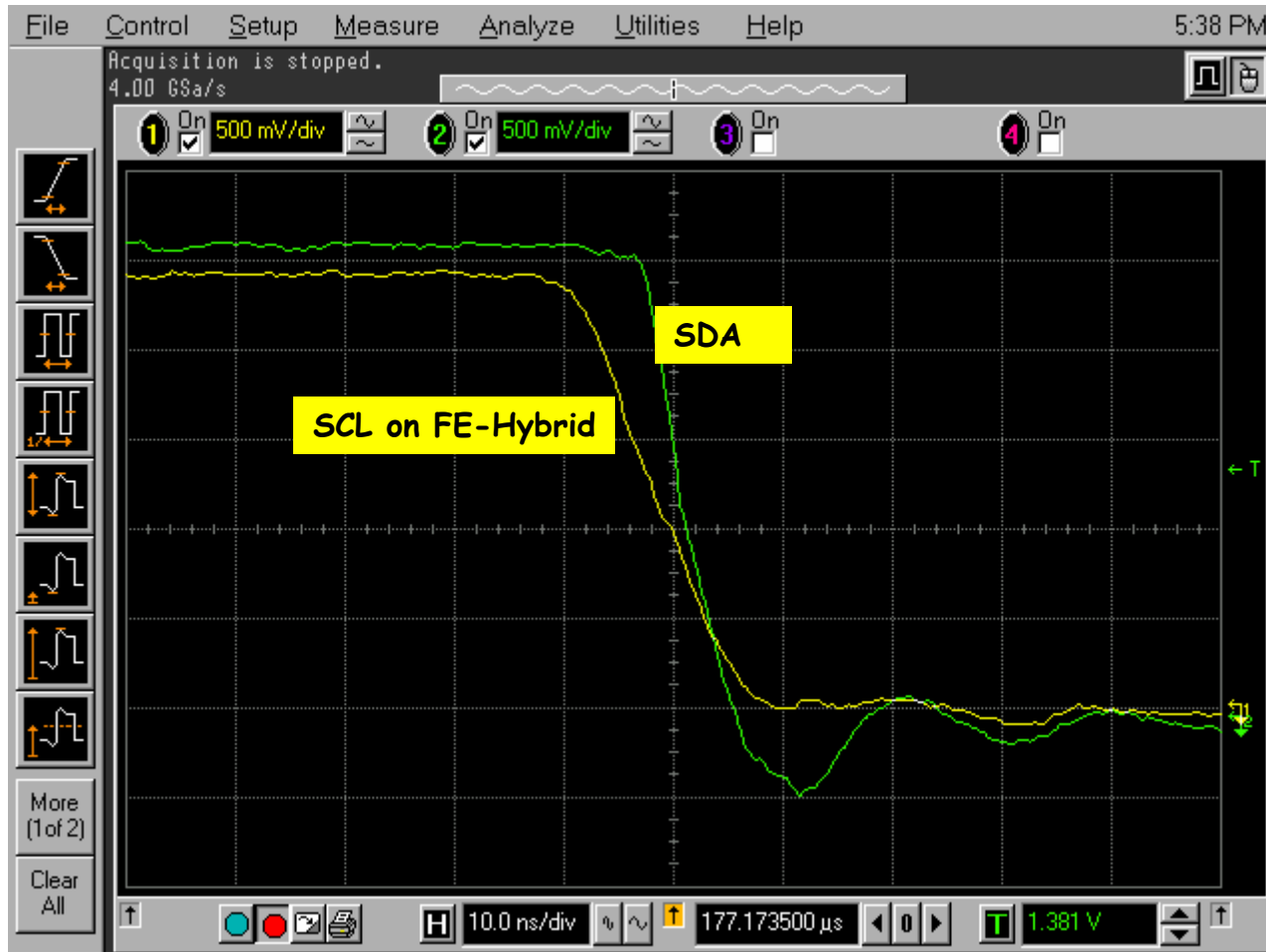


Example for an I2C write cycle

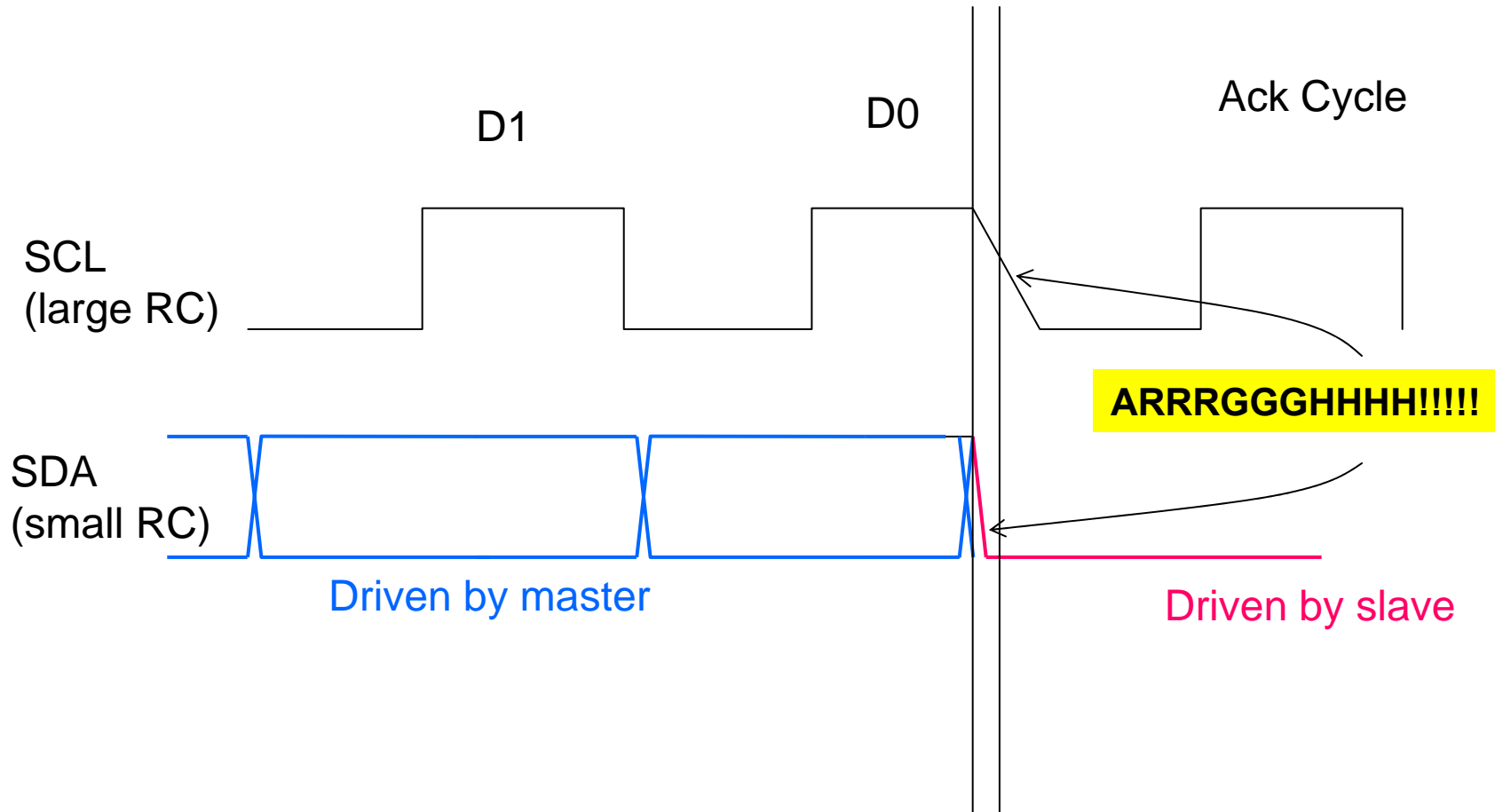
The actual waveforms



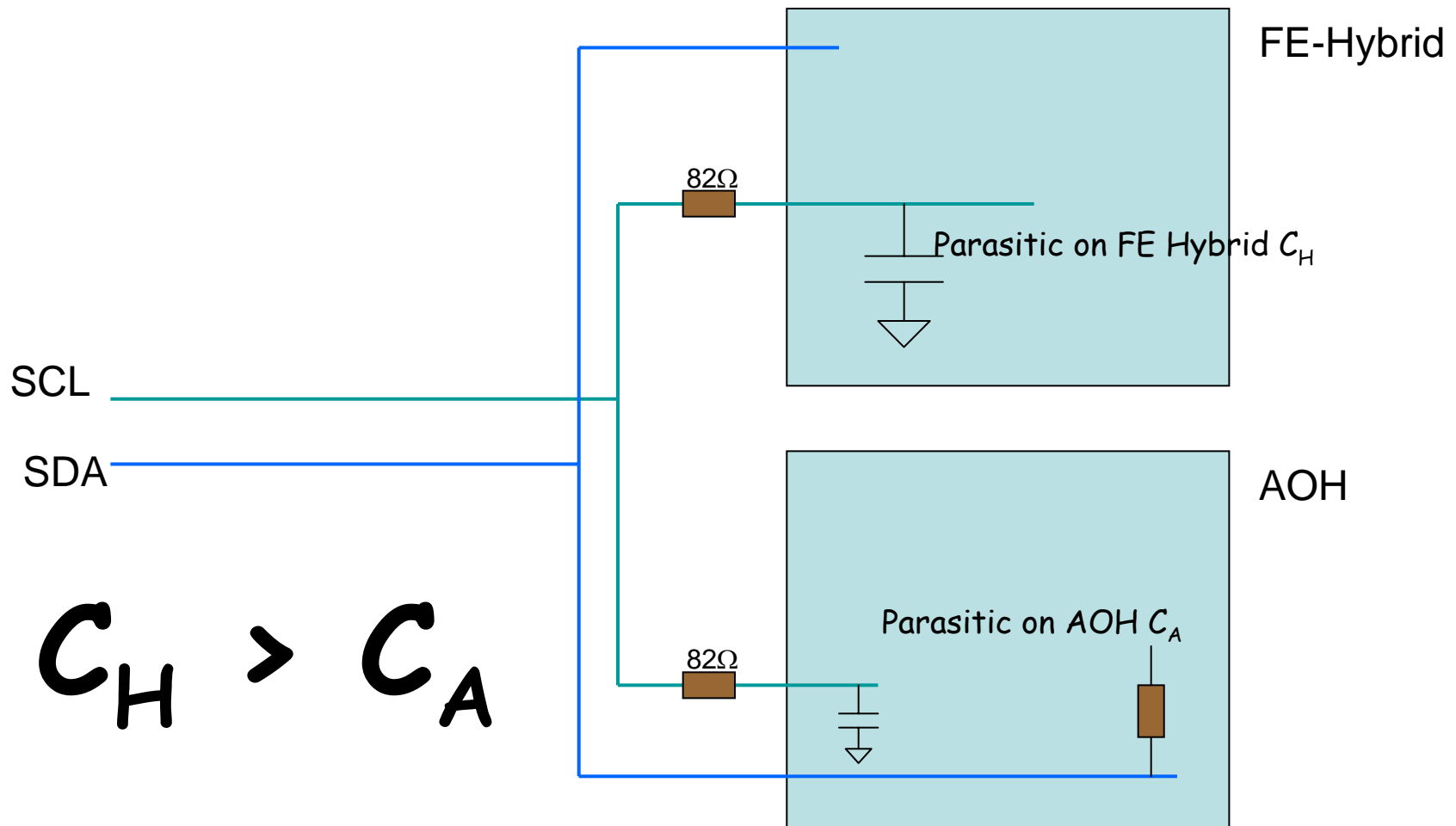
... on scope



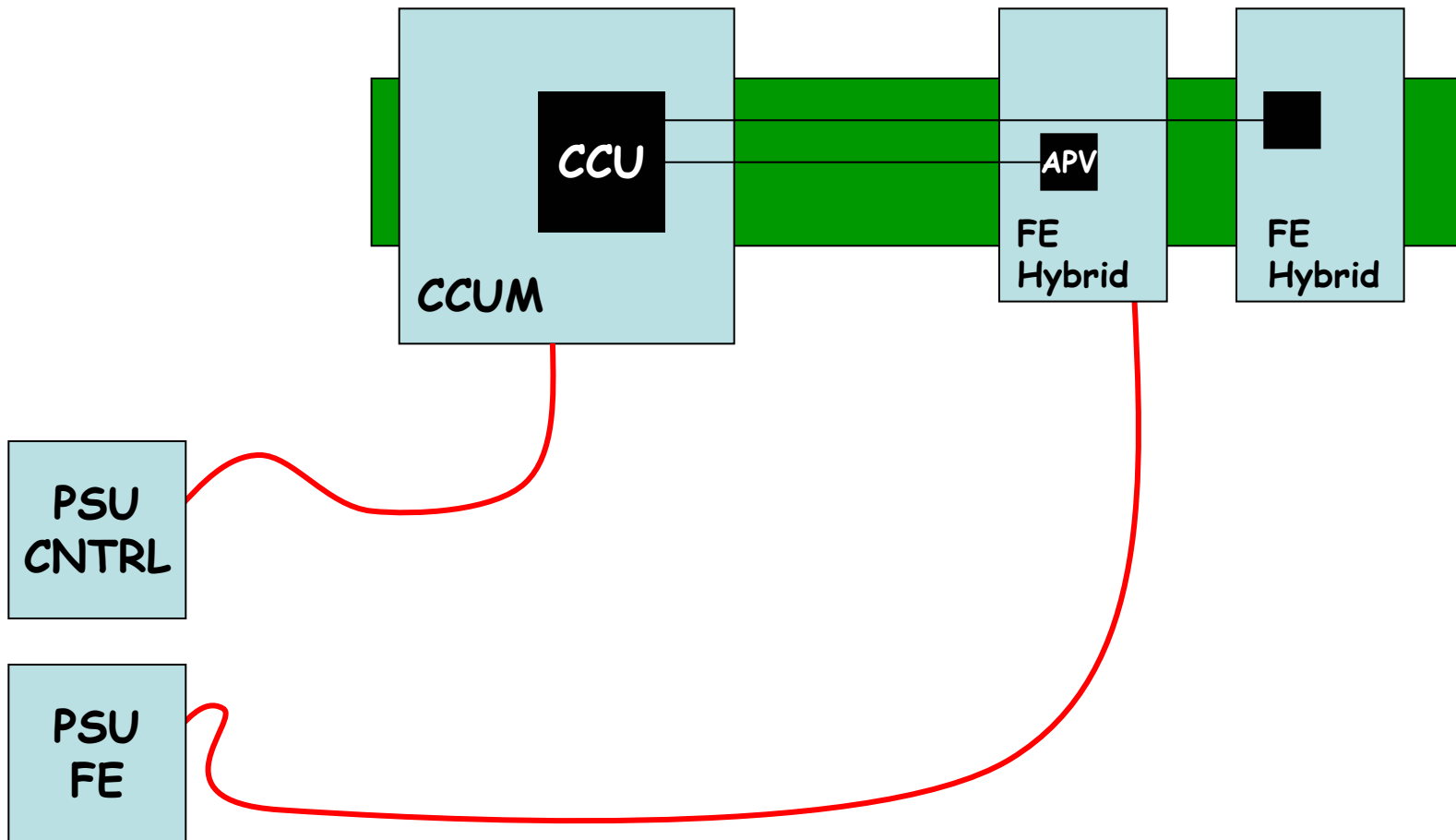
What we believe the APV believes



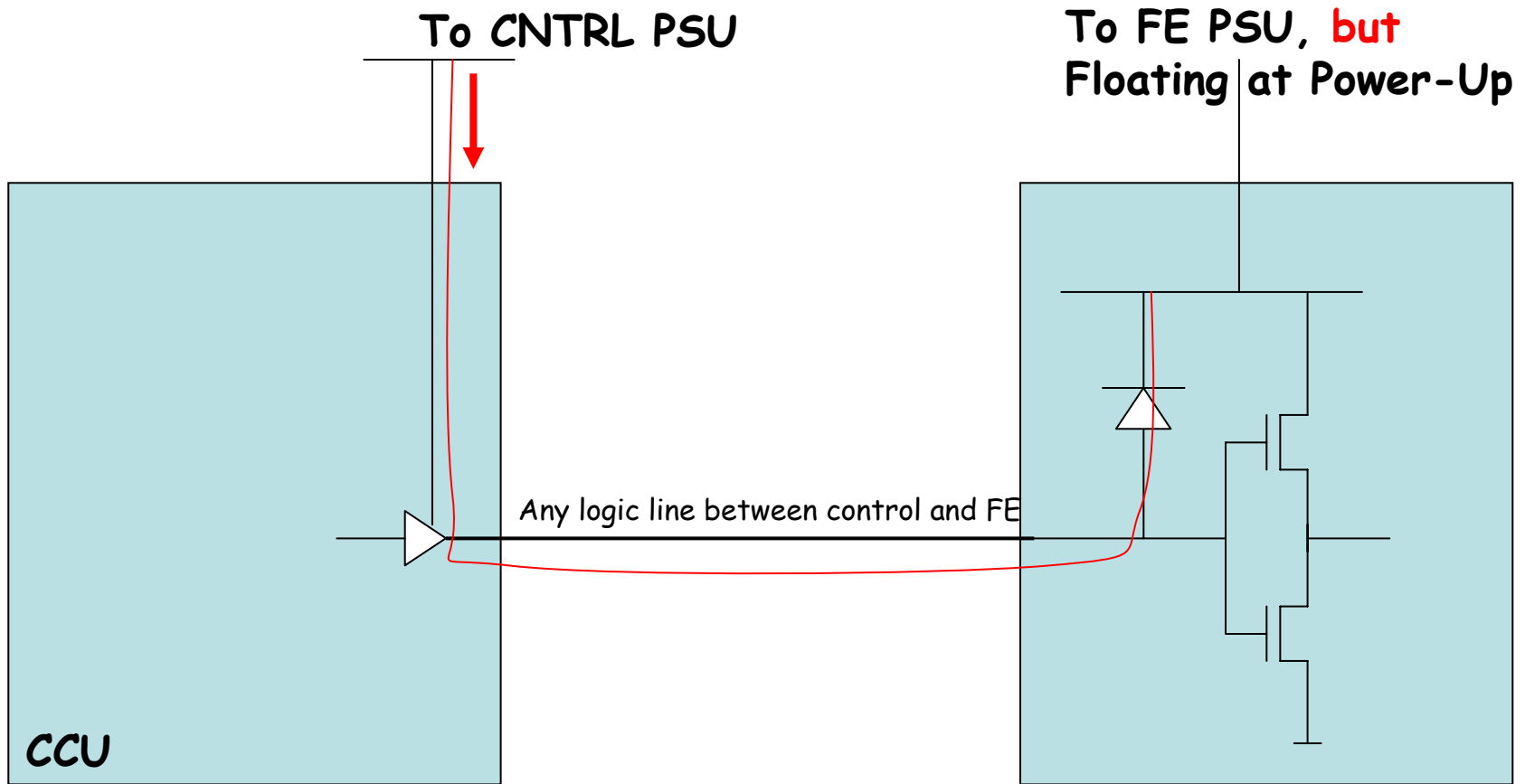
Present Electrical circuit



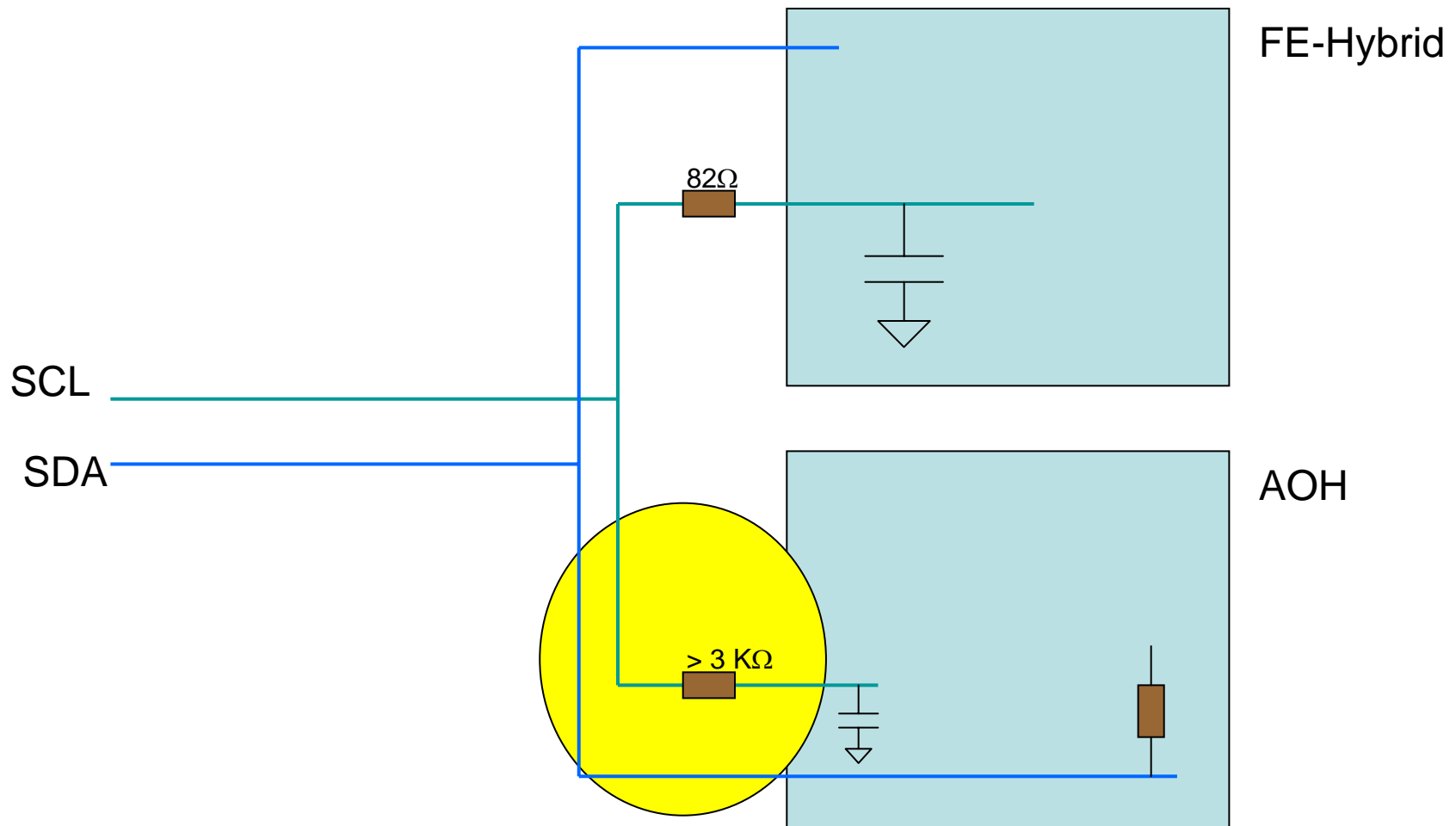
Why were resistors added?



Why are resistors added ? (2)



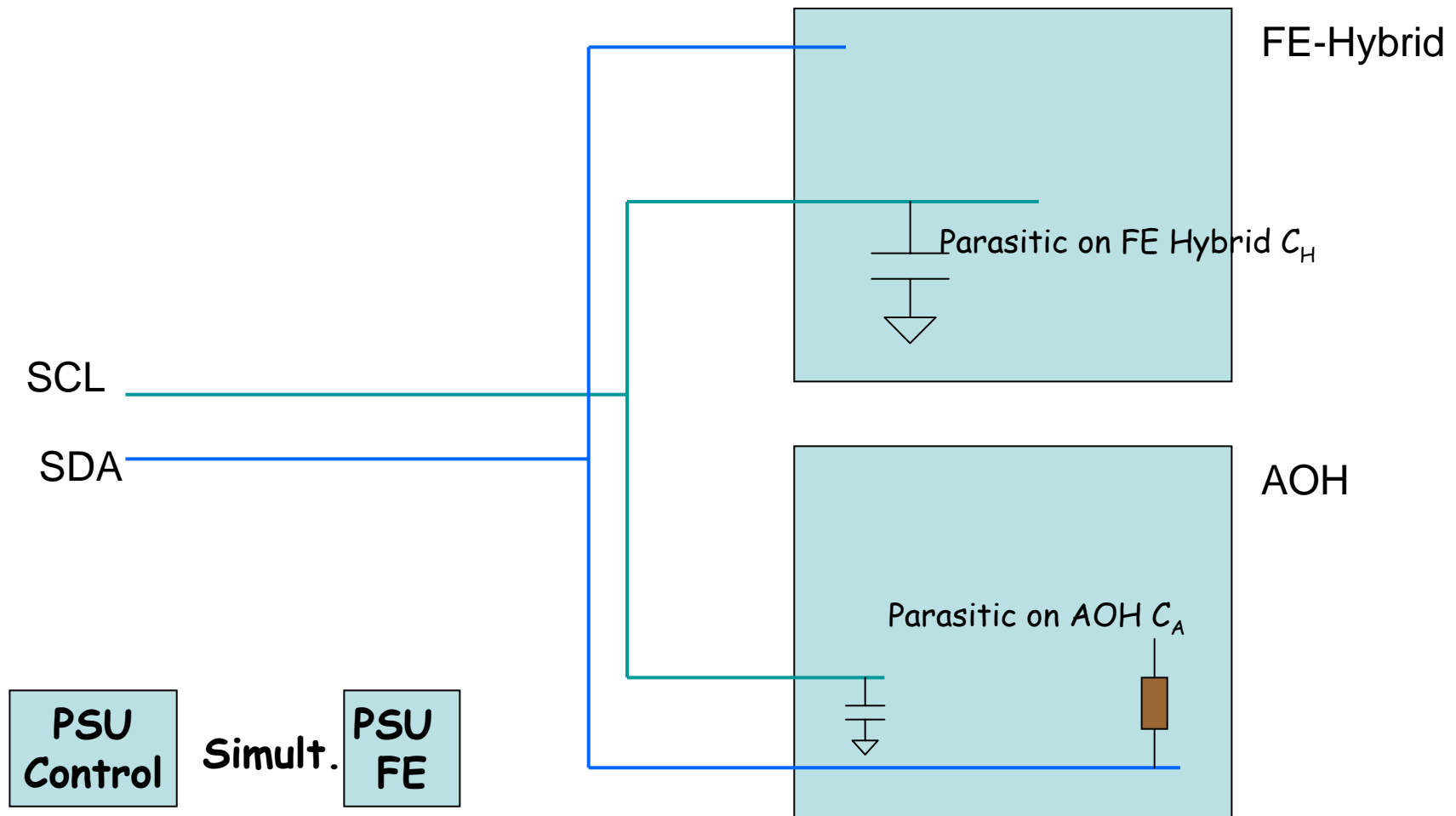
"Simple" Circuit equalization



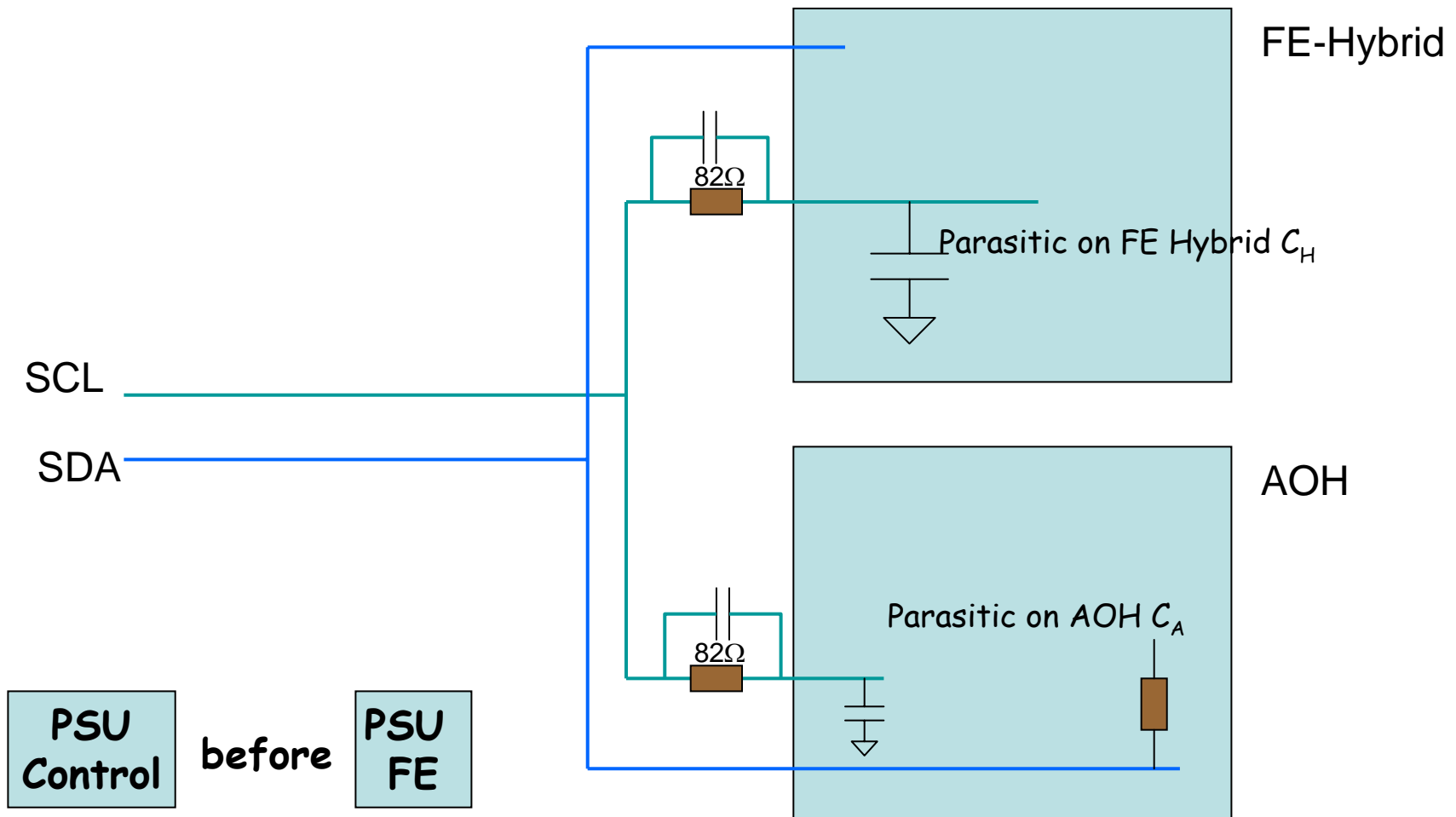
Possible solutions

1. Remove all protection resistors as to avoid different RC constants on ROD traces and introduce strict powering sequences
2. Use Wacek's ~ 2 nF bypass capacitor on resistors as to speed-up slow RCs edges
3. Tune Rs on different I2C traces as to guarantee correct SCL arrival time
4. Remove all resistors and introduce active protection to avoid short circuiting the CCUs to the FE during power-up
5. Remove resistors (same as 1.) and use only one power supply for CCUMs and FE hybrids
6. Short circuit I2C (SCL and SDA) lines after protection resistors, thus "equalizing" delay paths to AOH and APVs

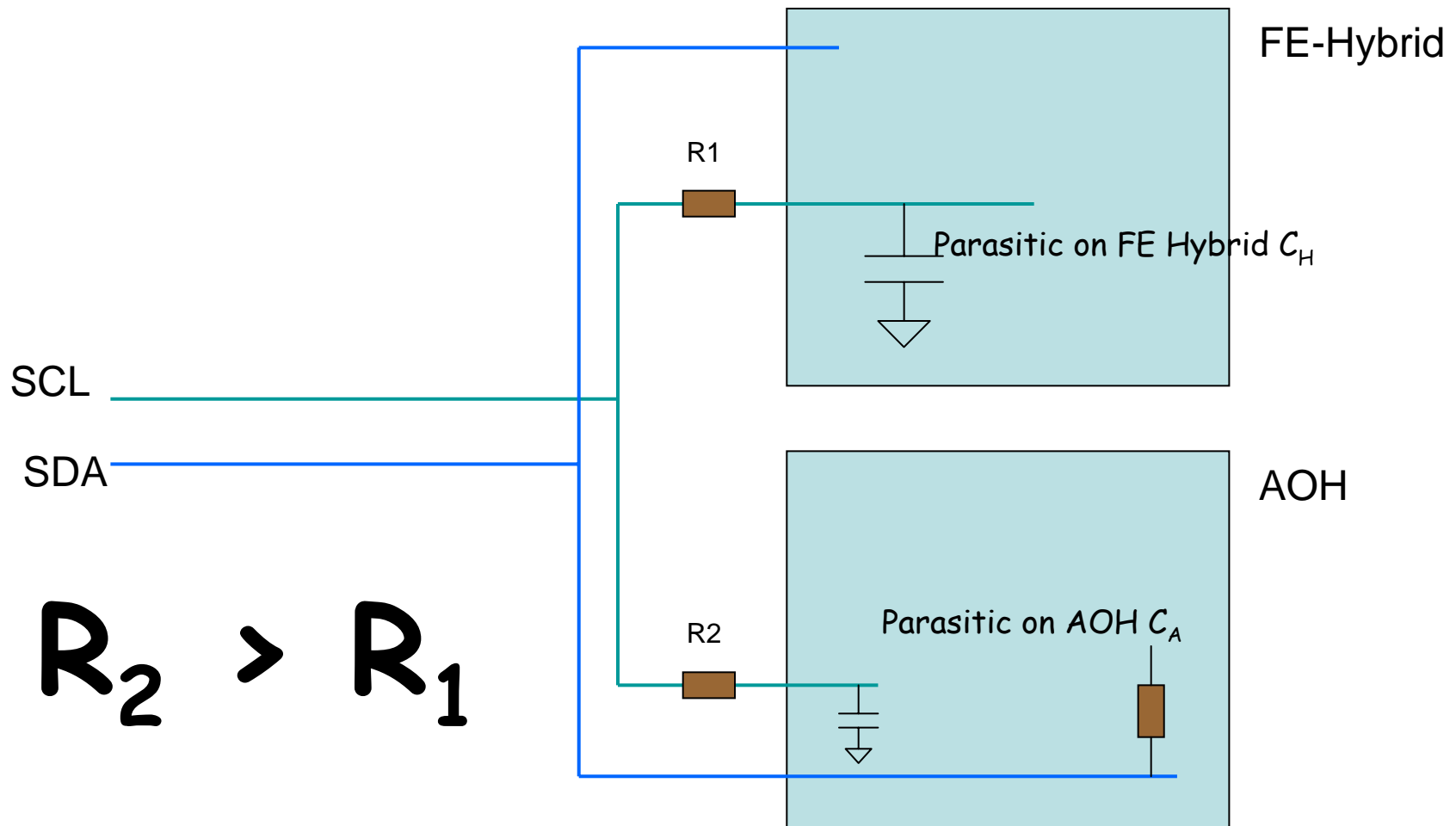
Solution 1



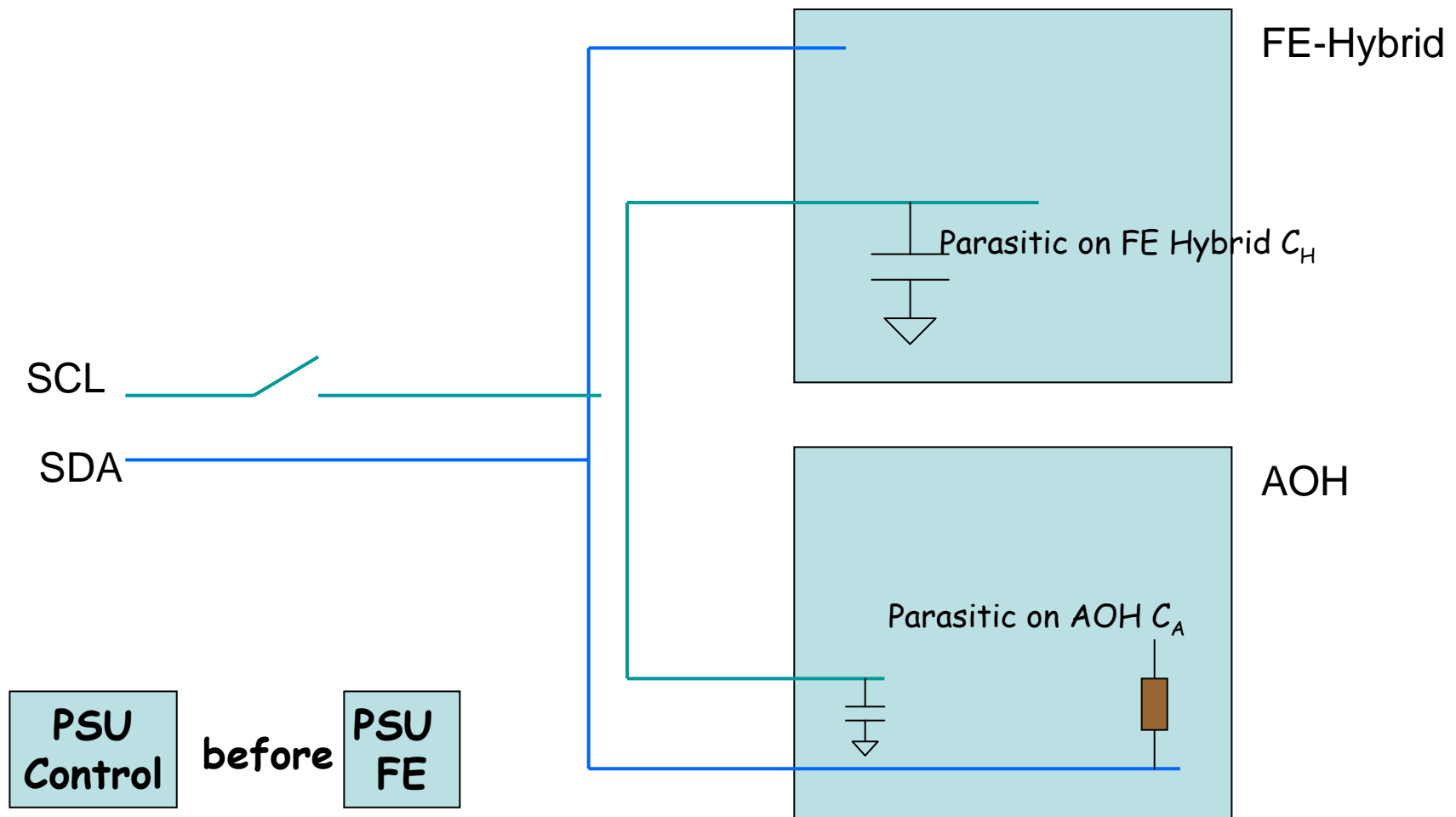
Solution 2



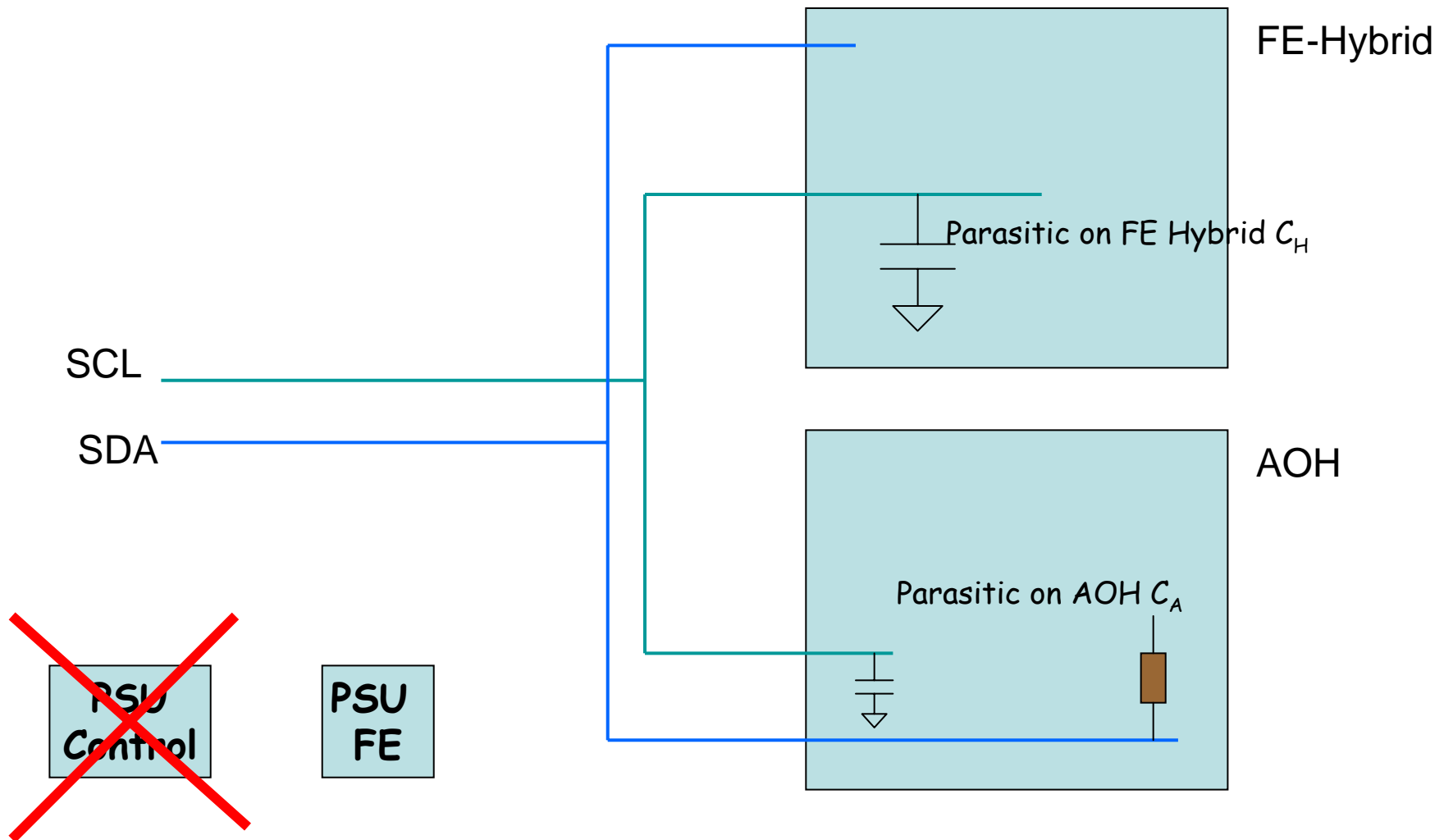
Solution 3



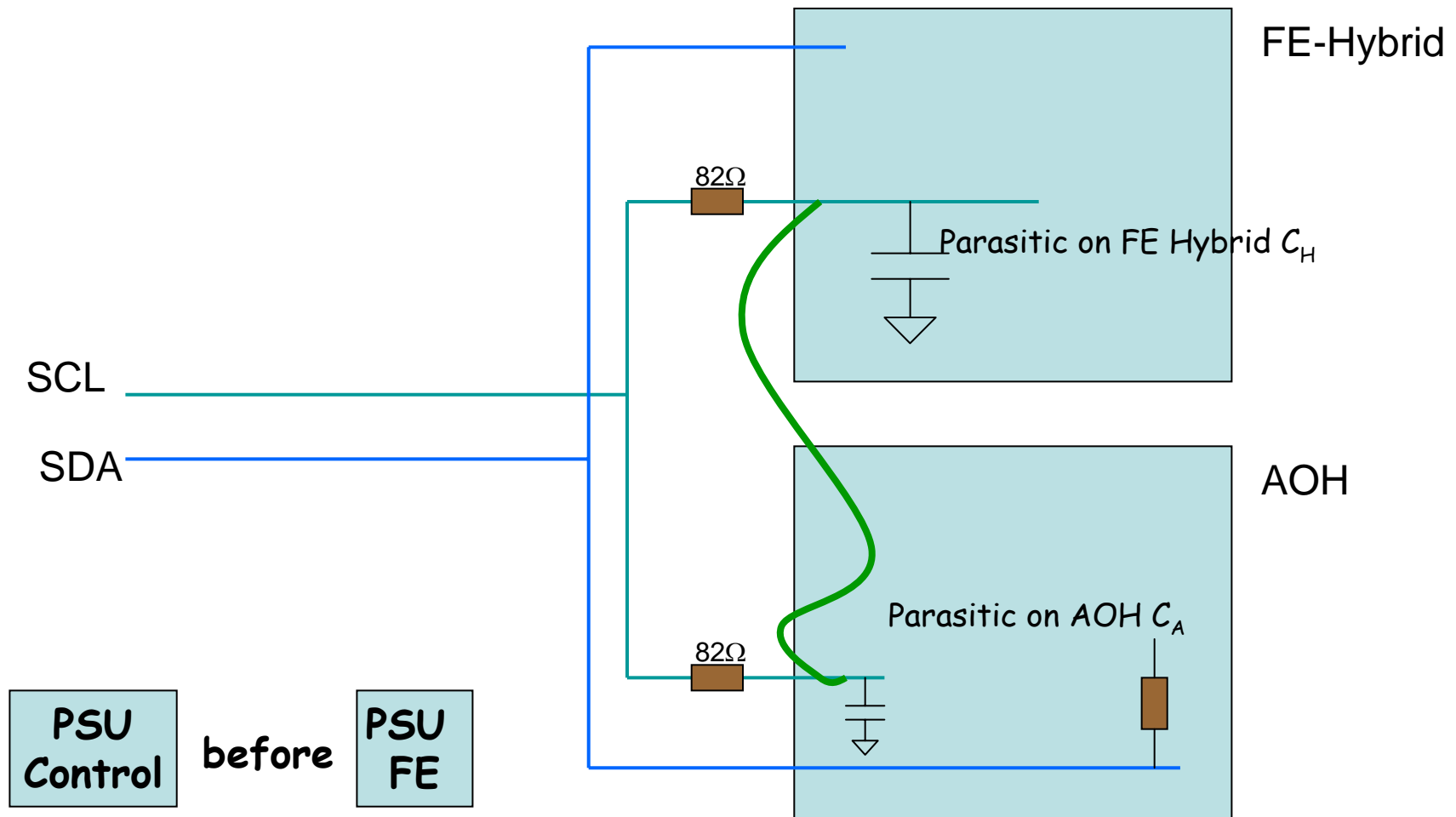
Solution 4



Solution 5



Solution 6



Comparison

	Pro	Con
1	- Works fine, no cumbersome tuning required	- Power sequence could be critical (potentially dangerous if power-up sequence control is lost) - Requires mod of all interconnect cards
2	- Well proved in Aachen	- Requires mod of all interconnect cards
3	- Seems to work	- Requires mod of all interconnect cards - Not obviously scalable, may require individual tuning of Rs
4	- Safe and robust	- Requires redesign and replacement of 700 CCUMs - Requires mod of all interconnect cards
5	- Works fine, no cumbersome tuning required - Saves money of control PSUs	- Careful about introducing digital noise - Requires minor mod to CCUM cabling - Possibly applicable only to TOB (DOHM cabling?) - Requires mod of all interconnect cards
6	(- This is how it should have been designed from the beginning)	- It would probably be best to eliminate the "T" altogether and have just one protection resistor - Requires mod of all interconnect cards

C ev! 5'

Marvin Johnson
Guido Magazzu'
Sandro Marchioro
Mark Raymond
Slawek Tkaczyk

Summary of Status

- The test systems in FNAL and S.Barbara have shown that (rarely) the I2C between CCUM and FEH and/or AOH can generate errors
- This was traced back to a timing problem occurring under certain conditions on the I2C bus
- The two signals on the bus (SCLK (i.e. clock) and SDA (i.e. data) are not properly propagated electrically along the TOB control chain: CCUM->ICC->Hybrid

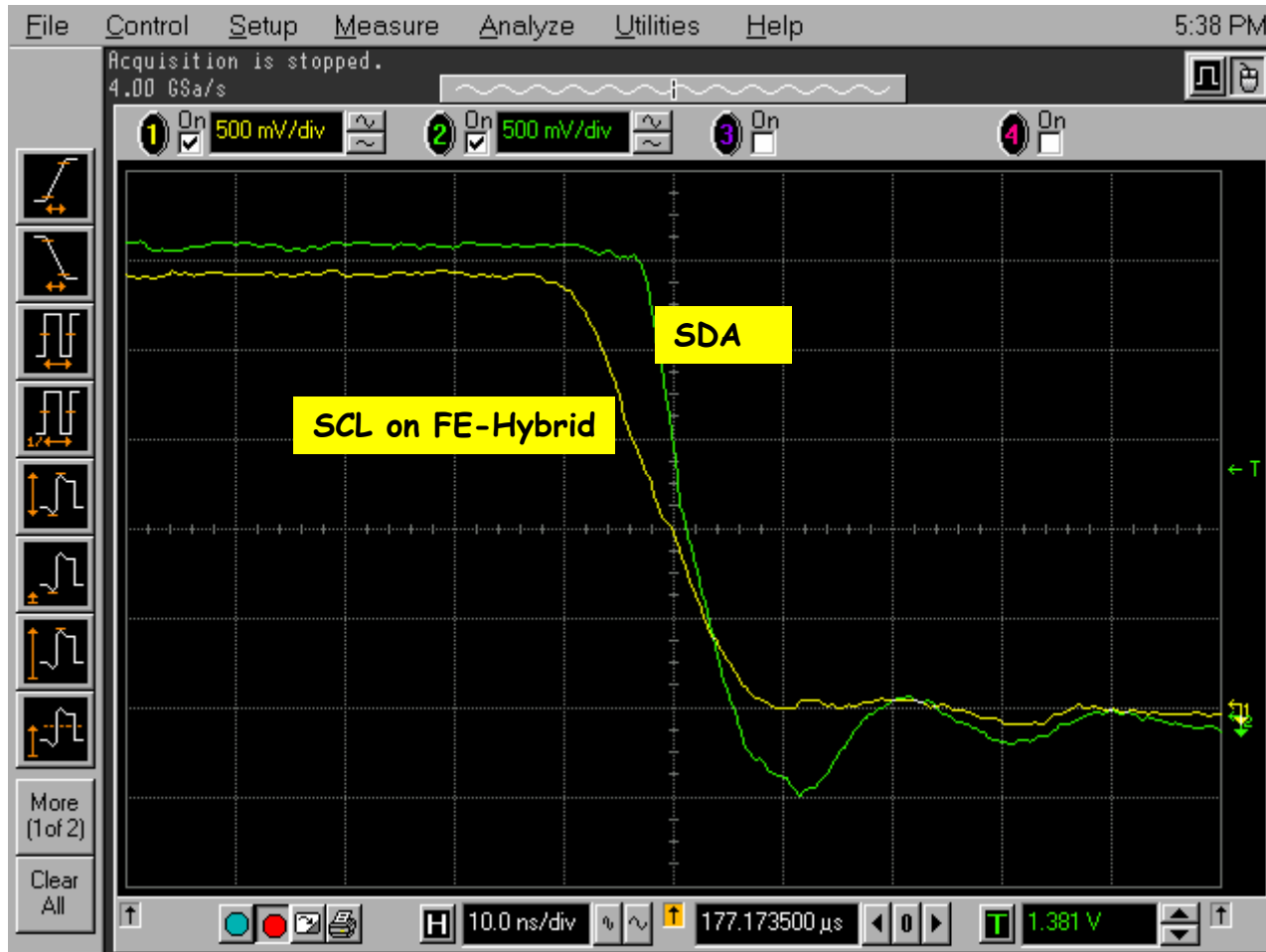
Situation as from last week

- A number of potential fixes (actually 6) have been proposed
 - All of them have good and bad features, there is no single fix that offers at the same time :
 - Robustness (i.e. large operating margin)
 - Simplicity (i.e. some work is always required)
 - Low cost
 - Small impact on TOB construction

Summary of possible Fixes

1. Remove all protection resistors as to avoid different RC constants on ROD traces and introduce strict powering sequences
2. Use Wacek's ~ 2 nF bypass capacitor on resistors as to speed-up slow RCs edges
3. Tune Rs on different I2C traces as to guarantee correct SCL arrival time
4. Remove all resistors and introduce active protection to avoid short circuiting the CCUs to the FE during power-up
5. Remove resistors (same as 1.) and use only one power supply for CCUMs and FE hybrids
6. Short circuit I2C (SCL and SDA) lines after protection resistors, thus "equalizing" delay paths to AOH and APVs
7. To be introduced today

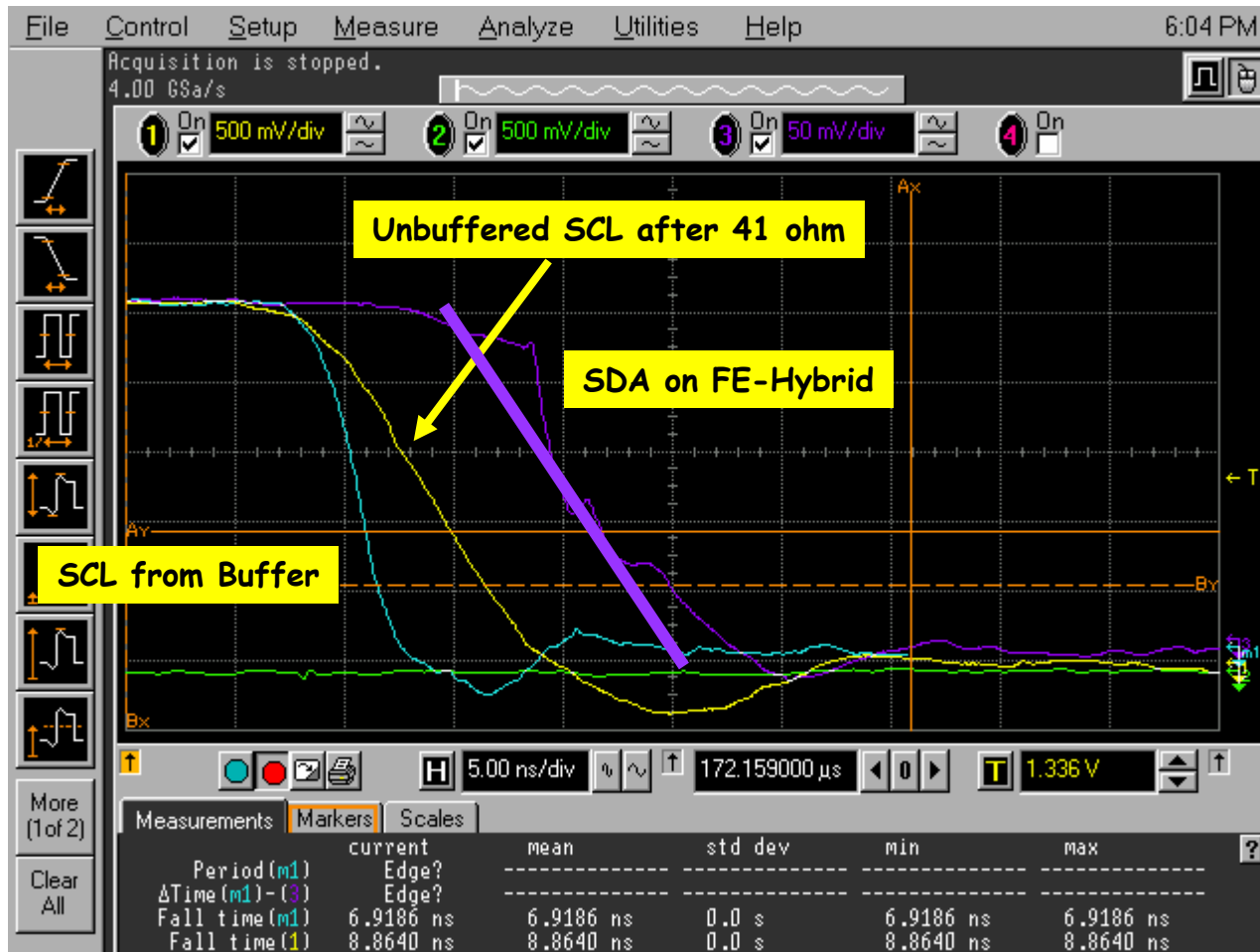
What are we fighting



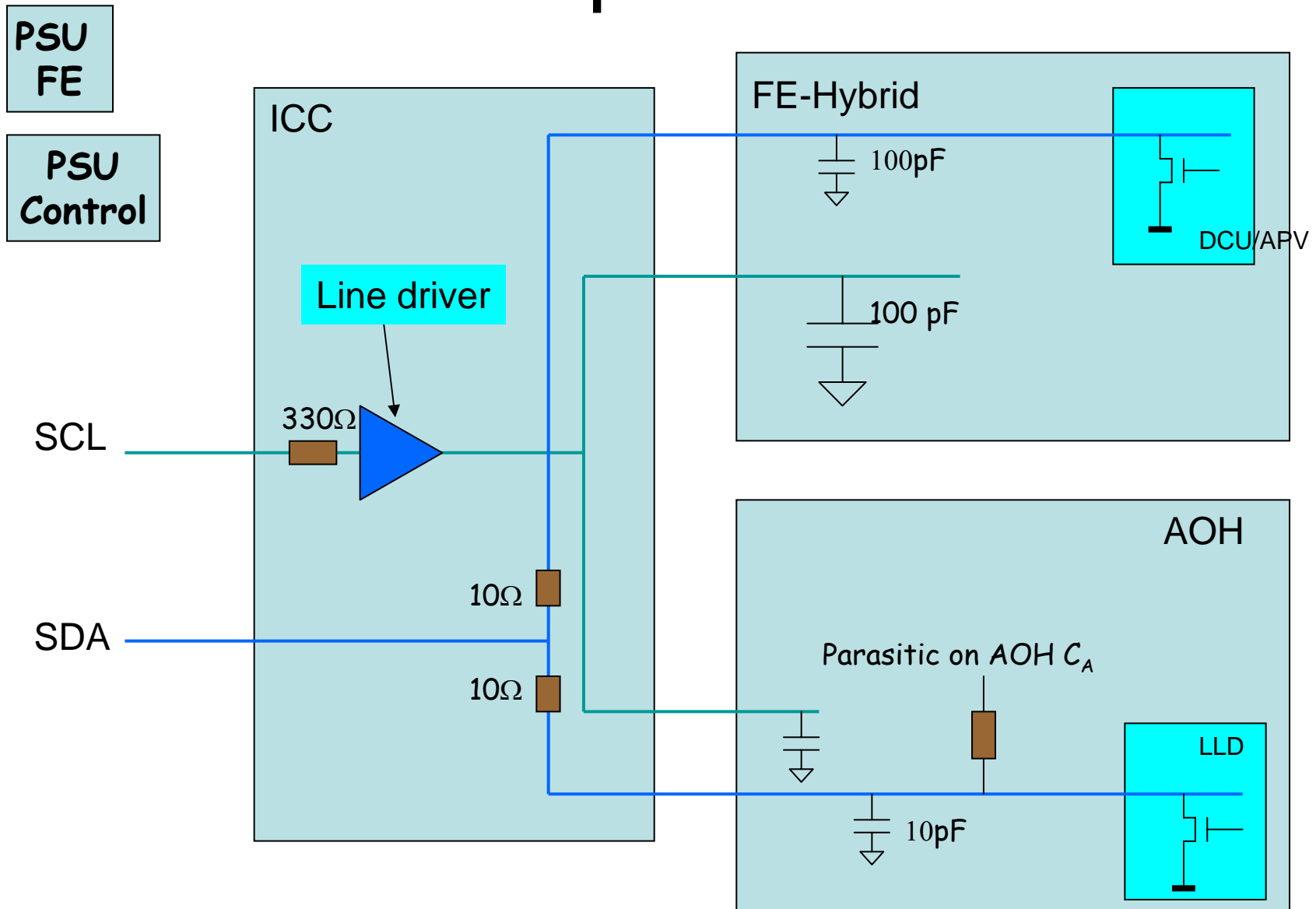
How does the problem arise

- Through a combination of:
 - Minor weaknesses in implementation of I2C protocol
 - Unfortunate choice of layout in interconnect card (“T” line layout instead of linear transmission line)
 - High capacitance of FE hybrid
 - Improper choice of inductive signal transmission in Kapton pig-tail on FE hybrid
- It results in:
 - Unsafe timing margin between SCL and SDA line as seen on FEH and/or AOH,
 - to make things worse this is (I2C) data dependent

Safety Margin



Option 7



Plan for action

- Complete construction of 30-50 RODs using the previously proposed solution “6” (i.e. short the SCL line on the ICC card after protection resistor)
- Instrument a sector of the TOB with these RODs and proceed as speedily as possible with the verification of all the other aspects of operating a reasonably large number of RODs (e.g. cross-talk, grounding, etc.)
- In parallel, and to strengthen understanding of system, a better ICC has to be built:
 - Redesign complete/partial lot of ICC to support the more robust solution 7
- I2C behavior on TEC and TIB should be verified with the same level of accuracy

Plan for implementation of solution 7

- A new proto series of ICC is absolutely necessary to study and digest in details several not yet completely understood effects
 - Measurements of GHz effects on small cards, with flying wires, with small chips and no test point are difficult and error-prone
 - New layout of 4 different card types (but with priority on the single type of card that has actually given problems in module 6 and 4)
 - Fabrication of films
 - Assembly of Prototypes:
 - Series of some 10 cards each
 - Mounting of 10 cards
 - Entire Lot:
 - Acquire components (critical are the NAIS connectors)
 - Testing
-

Cost

- The cost of the previous fabrication lot of ICC cards was ~ 108 KCHF
- Some money can be saved out of experience
- Some money must be added to speed out handling of “urgent” lot