I2C Signal propagation on TOB cards Where do we stand

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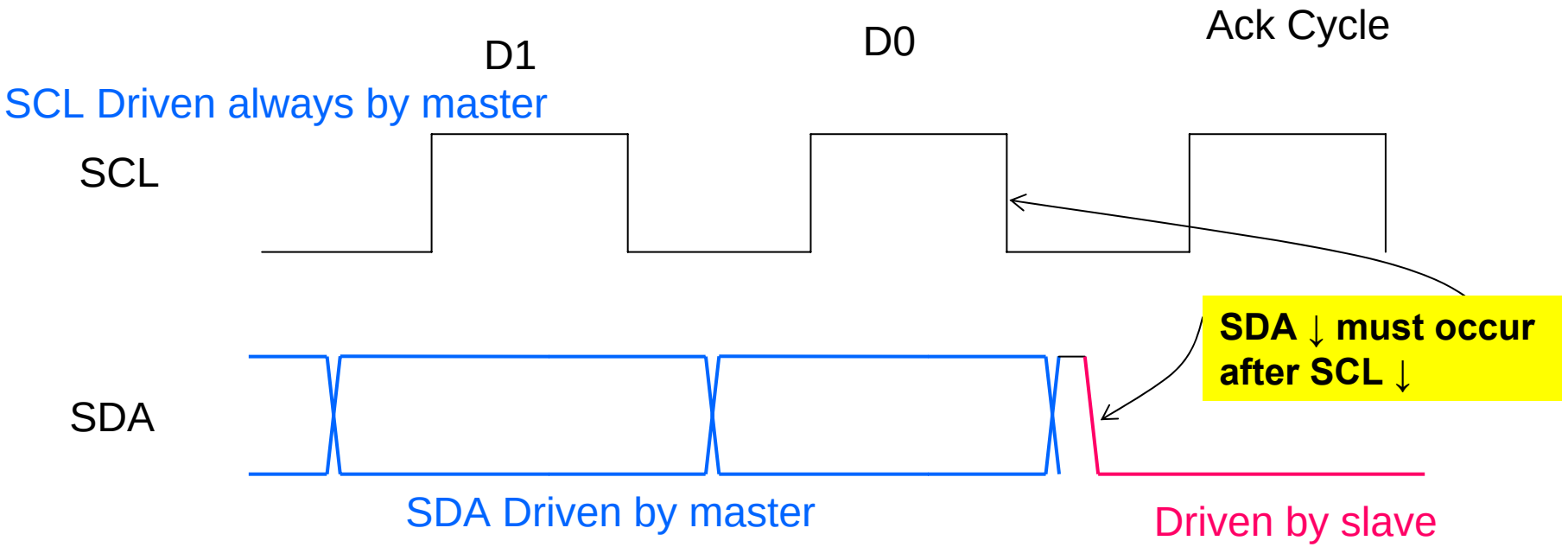
The simplified facts

- Occasionally, when accessing sequentially components on the I2C bus (LLD, DCU etc.), the APVs are found not to respond correctly to I2C commands

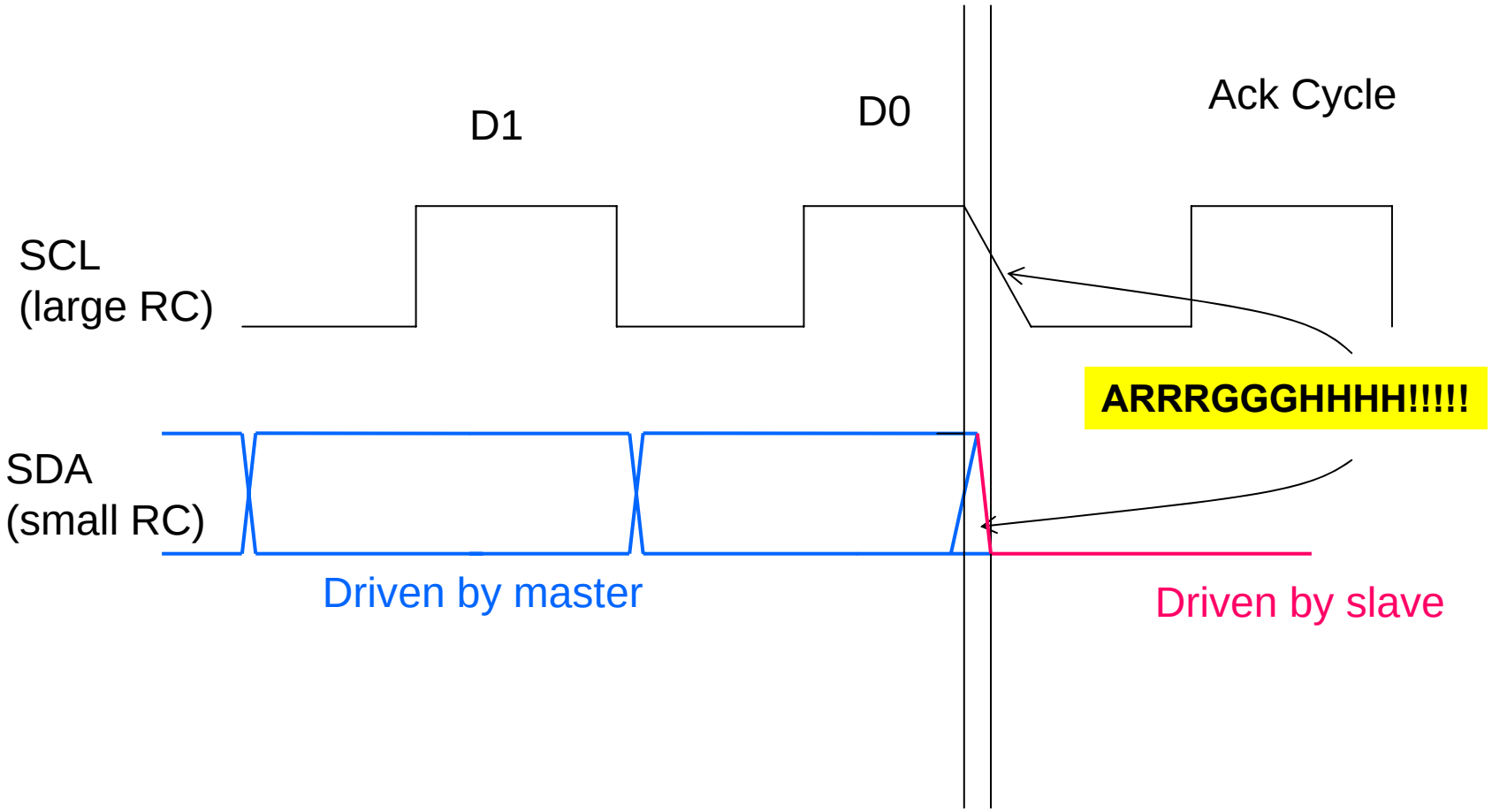
- This can data pattern dependent (as the last bit of the data sequence is the one most often misinterpreted)

The theoretical waveforms

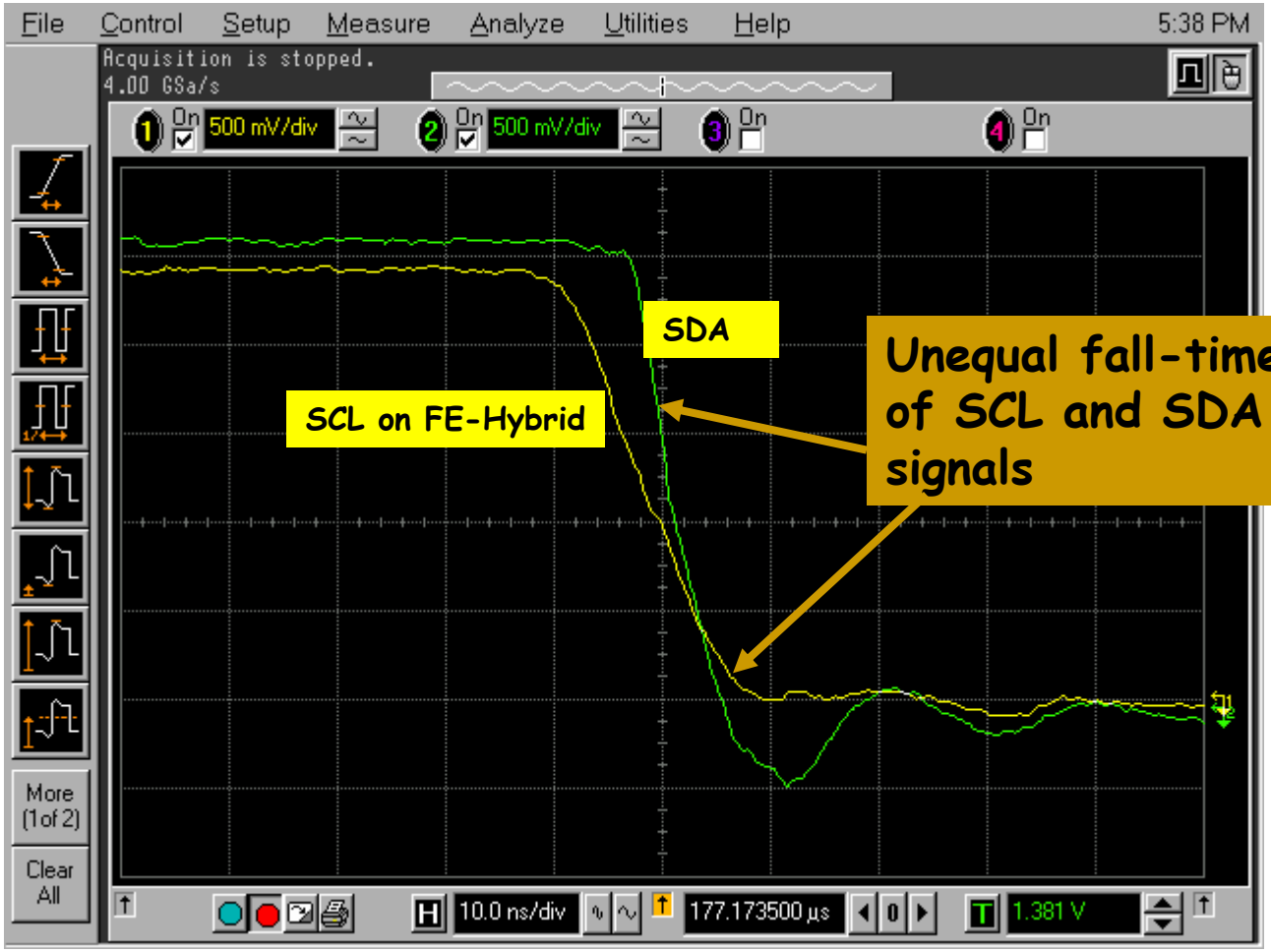


Example for an I2C write cycle

The actual waveforms



Main cause



Picture shows sequence of SCL/SDA signals with SDA pulled-down in AOH and measured on FEH

Additional info (13/7/05)

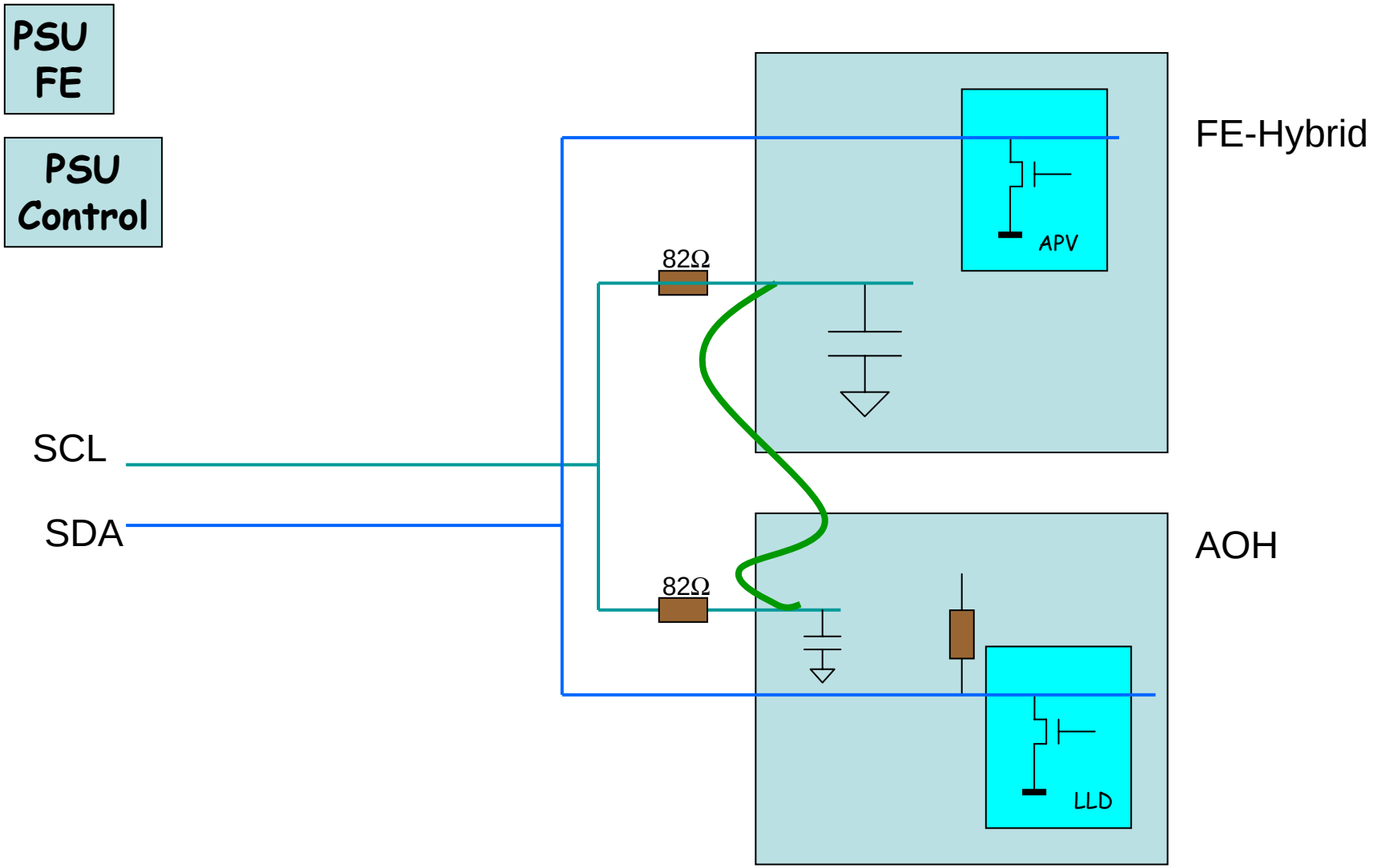
1. TEC has no problem with the "Karpinski" solution, should stay with it !
2. TIB has run numerous and exhaustive tests on communication protocol on small and large setups and they do not report any problem: Their HW corresponds to version '0' of the design, i.e. no "T" on the SCL line and single well terminated line
3. (98% CF) St. Barbara and FNAL have no problem even in the cold with the "jumper" solution, but several other I2C problems are present probably due to imperfect software

Remaining solutions

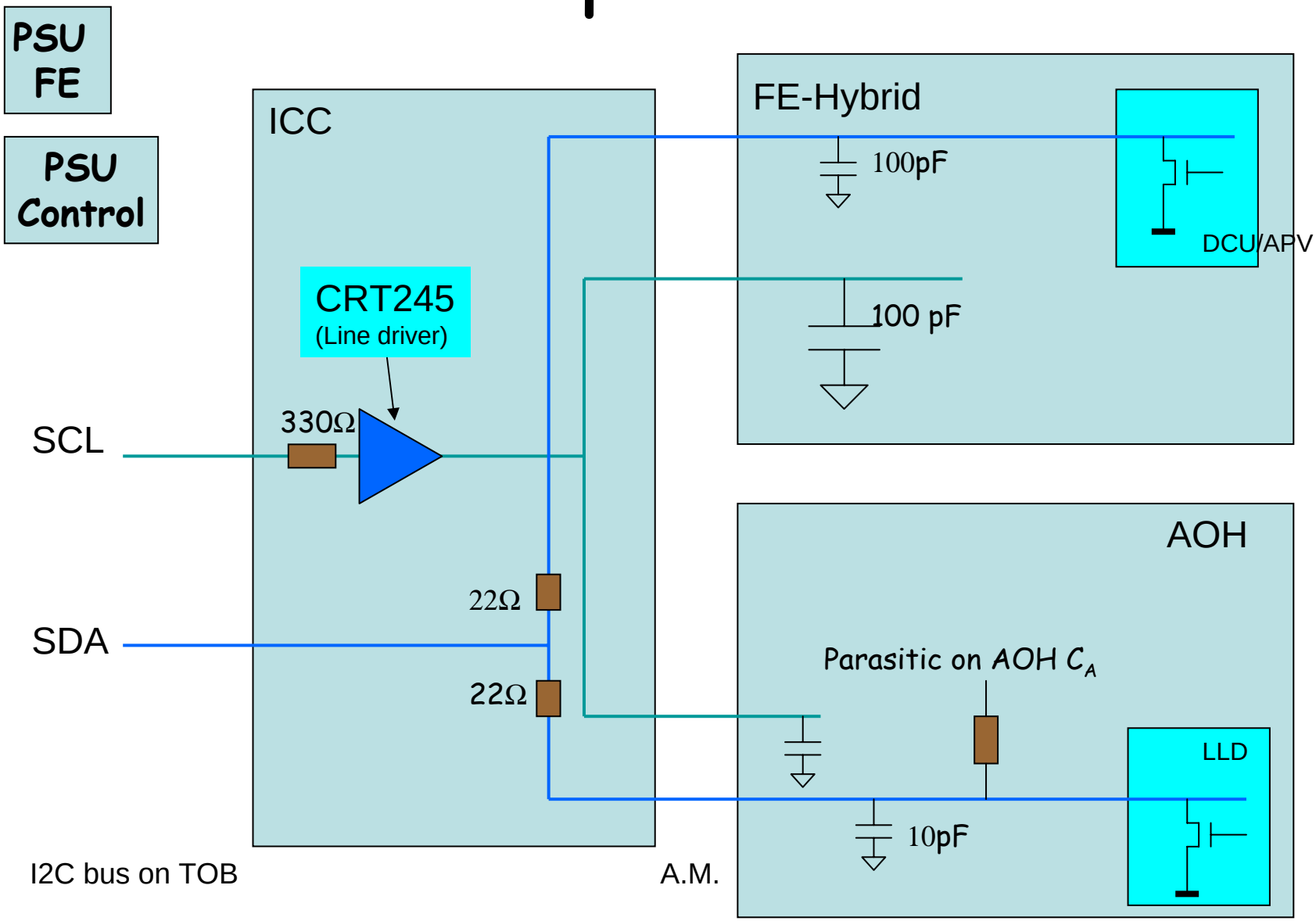
Solution 1 to 5

DISCARDED

Solution 6



Option 7


PSU FE
PSU Control
ICC
FE-Hybrid
100pF
DCU/APV
CRT245
(Line driver)
100 pF
330Ω
SCL
22Ω
SDA
22Ω
AOH
Parasitic on AOH C_A
LLD
10pF

Effect of "damping" resistor

SCL not show on this slide

Comparison of Options

"Jumper" (solution 6)	"Buffer on SCL line" (solution 7)
Simple and proved to work in FNAL and St. Barbara	Additional timing margins added: -Cleaner signal from buffer(<1 ns) -"Damping" resistors (~5 ns)
	Less current drawn from control PSU
	"Beneficial Collateral" card change on card wings allows possible grounding of ICC to cooling pipes (if necessary)
	Costly (time & money)

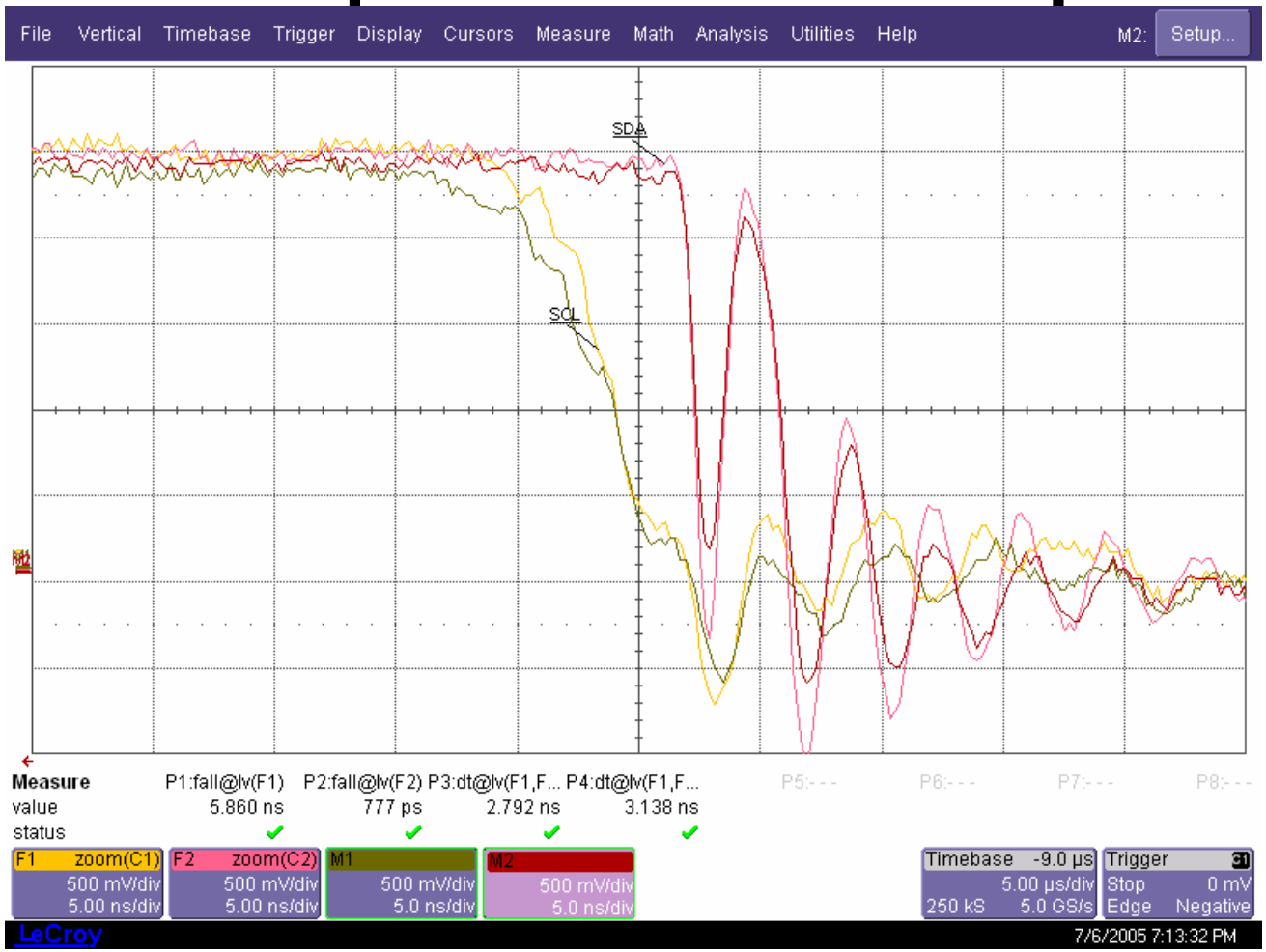
A word of caution

- Timing margin can change due to:

Process variation	All chips produced in same batch, very small variation
Temperature	Very noticeable (see following slides)
Irradiation damage	Measured effect is only 5-8 %

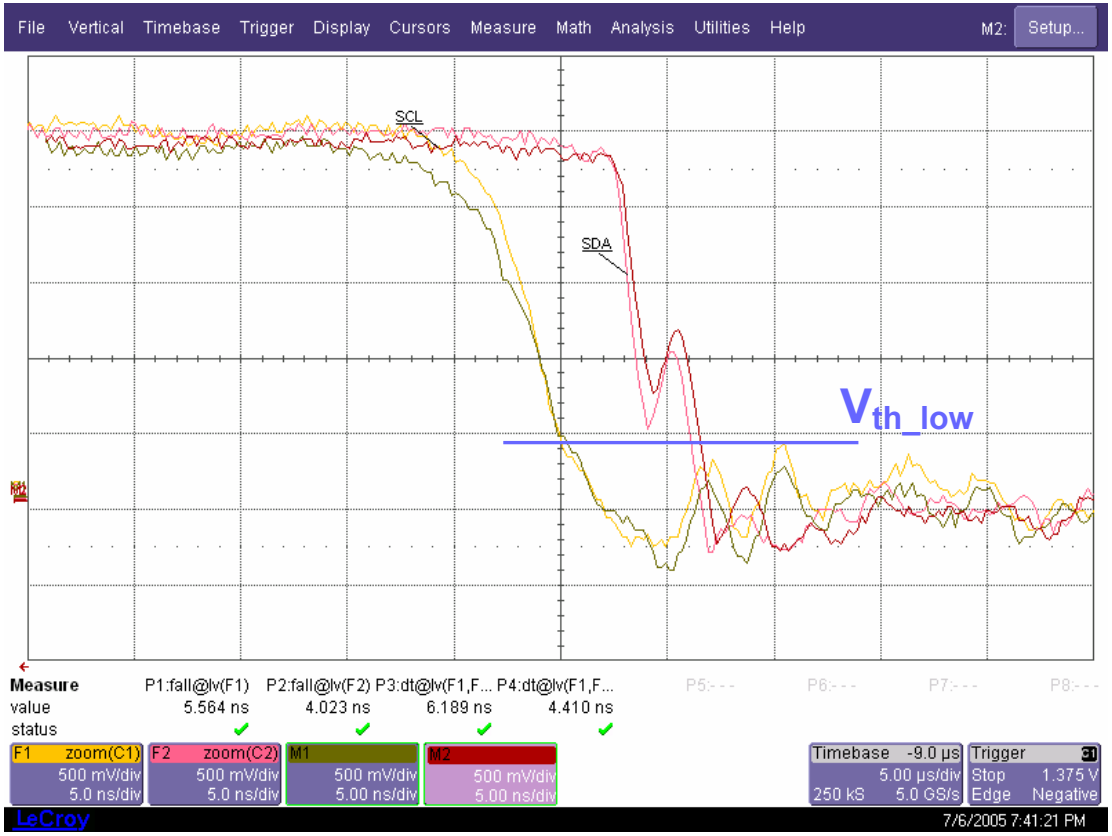
- Supply voltage changes can always be compensated for !

Temperature comparison (1)



Pos. 42 LDD response measured on the AOH at -23°C and at RT

Temperature comparison (2)



Pos. 42 LDD response measured on the FEH at -23°C and at RTW.
Karpinski-Aachen

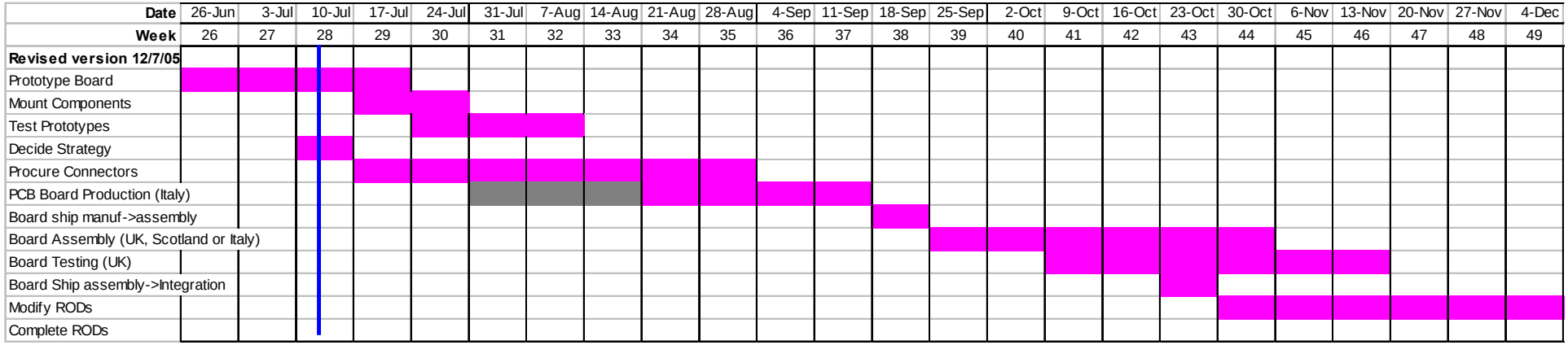
What to do next with the constraint of generating a minimum of impact on the TOB construction ?

Plan for action

1. Complete construction of 30-50 RODs using the proposed solution "6" (already approved !)
2. Instrument a sector of the TOB with these RODs and proceed as speedily as possible with the verification of all the other aspects of operating a reasonably large number of RODs, e.g. cross-talk, grounding, etc. (already approved !)

3. In parallel, and to strengthen understanding of system, a better ICC has to be built:
    1. Redesign lot of ICC cards to support the more robust solution 7
4. I2C behavior on TEC and TIB should be verified with the same level of accuracy

Schedule



Assumptions:

- The 4 different ICC cards are made in two lots of two
- Order for PCB production must be in Italy by July 29th
- Order for Assembly must be with manufacturer by July 29th
- Written detailed commercial and technical offers still NOT available

Cost

- Connectors are cheaper than two years ago
- The total foreseen cost is ~ 100 KCHF
- …but an accelerated schedule may require some extra $$$