I2C Signal propagation on TOB cards
Where do we stand

A. Marchioro
13/7/2003 v.2
The simplified facts

- Occasionally, when accessing sequentially components on the I2C bus (LLD, DCU etc.), the APVs are found not to respond correctly to I2C commands.

- This can data pattern dependent (as the last bit of the data sequence is the one most often misinterpreted).
The theoretical waveforms

Example for an I2C write cycle

SCL Driven always by master

SDA Driven by master

D1

D0

Ack Cycle

SDA ↓ must occur after SCL ↓

Driven by slave
The actual waveforms

I2C bus on TOB

A.M.
Main cause

Picture shows sequence of SCL/SDA signals with SDA pulled-down in AOH and measured on FEH.

Unequal fall-time of SCL and SDA signals.
Additional info (13/7/05)

1. TEC has no problem with the “Karpinski” solution, should stay with it!
2. TIB has run numerous and exhaustive tests on communication protocol on small and large setups and they do not report any problem: Their HW corresponds to version ‘0’ of the design, i.e. no “T” on the SCL line and single well terminated line
3. (98% CF) St. Barbara and FNAL have no problem even in the cold with the “jumper” solution, but several other I2C problems are present probably due to imperfect software
Remaining solutions
Solution 1 to 5

DISCARDED
Solution 6
Option 7

PSU FE

PSU Control

ICC

CRT245 (Line driver)

SCL

330Ω

22Ω

SDA

22Ω

A.M.

100 pF

100 pF

LLD

DCU/APV

AOH

Parasitic on AOH $C_A$

10 pF

I2C bus on TOB

PSU

FE

Control

CRT245 (Line driver)

22Ω

22Ω

330Ω

FE-Hybrid

AOH

LLD

DCU/APV

Parasitic on AOH $C_A$
Effect of “damping” resistor

SDA with “damping”

SDA without “damping”

SCL not show on this slide
## Comparison of Options

<table>
<thead>
<tr>
<th>“Jumper” (solution 6)</th>
<th>“Buffer on SCL line” (solution 7)</th>
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<tbody>
<tr>
<td>Simple and proved to work in FNAL and St. Barbara</td>
<td>Additional timing margins added: -Cleaner signal from buffer (&lt;1 ns) -“Damping” resistors (~5 ns)</td>
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<td>Less current drawn from control PSU</td>
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<td>“Beneficial Collateral” card change on card wings allows possible grounding of ICC to cooling pipes (if necessary)</td>
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<td>Costly (time &amp; money)</td>
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I2C bus on TOB

A.M.
A word of caution

- Timing margin can change due to:

<table>
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<th>Process variation</th>
<th>All chips produced in same batch, very small variation</th>
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<tr>
<td>Temperature</td>
<td>Very noticeable (see following slides)</td>
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<td>Irradiation damage</td>
<td>Measured effect is only 5-8 %</td>
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- Supply voltage changes can always be compensated for!
Temperature comparison (1)

Pos. 42 LDD response measured on the AOH at -23°C and at RT

I2C bus on TOB

A.M. W. Karpinski-Aachen 14
Temperature comparison (2)

Pos. 42 LDD response measured on the FEH at -23°C and at RTW.
Karpinski-Aachen
What to do next with the constraint of generating a minimum of impact on the TOB construction?
Plan for action

1. Complete construction of 30-50 RODs using the proposed solution “6” (already approved !)

2. Instrument a sector of the TOB with these RODs and proceed as speedily as possible with the verification of all the other aspects of operating a reasonably large number of RODs, e.g. cross-talk, grounding, etc. (already approved !)

3. In parallel, and to strengthen understanding of system, a better ICC has to be built:
   1. Redesign lot of ICC cards to support the more robust solution 7

4. I2C behavior on TEC and TIB should be verified with the same level of accuracy
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### Assumptions:
- The 4 different ICC cards are made in two lots of two
- Order for PCB production must be in Italy by July 29th
- Order for Assembly must be with manufacturer by July 29th
- Written detailed commercial and technical offers still NOT available
Cost

• Connectors are cheaper than two years ago
• The total foreseen cost is ~ 100 KCHF
• ...but an accelerated schedule may require some extra $$$