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ODMB user's manual

Optical DAQ MotherBoard for the ME1/1 stations of the CMS muon endcap detector

Firmware tag: V02-01

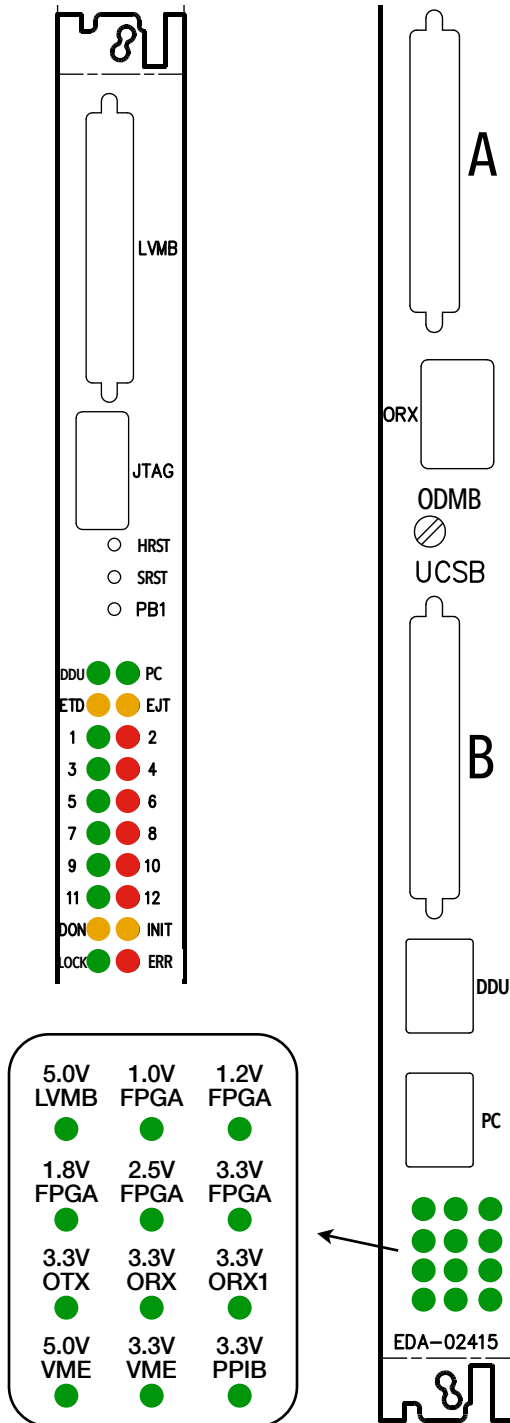
ODMB.V2 and ODMB.V3 compatible

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Front panel



Push buttons

- **HRST**: Reloads firmware in PROM onto FPGA
- **SRST**: Resets registers/FIFOs in FW. **LEDs 1-12** blink at different speeds for ~3s
- **PB1**: Sends L1A and L1A_MATCH to all DCFEBs. Turns on **LED 12**

LEDs set in firmware

- **1**: 4 Hz signal from clock for data → DDU
- **3**: 2 Hz signal from clock for data → PC
- **5**: 1 Hz signal from internal ODMB clock
- **7**: Data taking: ON normal, OFF pedestal
- **9**: Triggers: ON external, OFF internal
- **11**: Data: ON real, OFF simulated
- **2**: Bit 0 of L1A_COUNTER
- **4**: Bit 1 of L1A_COUNTER
- **6**: Bit 2 of L1A_COUNTER
- **8**: Bit 3 of L1A_COUNTER
- **10**: Bit 4 of L1A_COUNTER
- **12**: Briefly ON when a VME command is received. Also ON when **PB1** is pressed

LEDs set in hardware

- **DDU**: Signal Detected on DDU RX
- **PC**: Signal Detected on PC RX
- **ETD**: DTACK enable for discrete logic (active low)
- **EJD**: JTAG enable for discrete logic (active low)
- **DON**: DONE signal from FPGA. ON when programmed
- **INIT**: INIT_B signal from FPGA (active low)
- **LOCK**: QPLL is locked
- **ERR**: Error with QPLL
- **Bottom 12**: Voltage monitoring

General

Firmware version

For a given firmware tag **VXY-ZK**:

- ❖ Usercode is **XYZKdbdb**
- ❖ Firmware version read via "R 4200" is **XYZK**

VME access through the board discrete "emergency" logic

The FPGA may be accessed via JTAG through the discrete logic as follows

- ❖ The VME address is 0xFFFC
- ❖ The bit 0 of the data sent is TMS
- ❖ The bit 1 of the data sent is TDI

For example, to read the Usercode, starting from JTAG idle (five TMS = 1 & one TMS = 0), the commands are:

```

W FFFC 1 To Select-DR-Scan
W FFFC 1 To Select-IR-Scan
W FFFC 0 To Capture-IR
W FFFC 0 To Shift-IR

W FFFC 0 Shifting IR (Read UserCode IR = 3C8)
W FFFC 0 Shifting IR
W FFFC 0 Shifting IR
W FFFC 2 Shifting IR
W FFFC 0 Shifting IR
W FFFC 0 Shifting IR
W FFFC 2 Shifting IR
W FFFC 2 Shifting IR
W FFFC 2 Shifting IR
W FFFC 3 Shifting IR and to Exit1-IR

W FFFC 1 To Update-IR
W FFFC 0 To Run_Test/Idle
W FFFC 1 To Select-DR-Scan
W FFFC 0 To Capture-DR

W FFFC 0 Shifting DR
R FFFC 0 Shifting DR (Read bit 0 of UserCode)

```

Since the Usercode register is 32 bits, the last two commands should be repeated 31 more times.

Device 1: DCFEB JTAG

“Y” refers to the number of bits to be shifted

| Instruction | Description |
|---------------|---|
| W 1Y00 | Shift Data; no TMS header; no TMS tailer |
| W 1Y04 | Shift Data with TMS header only |
| W 1Y08 | Shift Data with TMS tailer only |
| W 1Y0C | Shift Data with TMS header & TMS tailer |
| | |
| R 1014 | Read TDO register |
| | |
| W 1018 | Resets JTAG protocol to IDLE state (data sent with this command is disregarded) |
| | |
| W 1Y1C | Shift Instruction register |
| | |
| W 1020 | Select DCFEB, one bit per DCFEB |
| R 1024 | Read which DCFEB is selected |

Example: Read DCFEB UserCode

DCFEB registers are set and read via JTAG. The following procedure reads the 32-bit USERID of DCFEB 3:

```

W 1020 4 Select DCFEB 3 (one bit per DCFEB)

W 191c 3C8 Set instruction register to 3C8 (read UserCode)
W 1F04 0 Shift 16 lower bits
R 1014 0 Read last 16 shifted bits (DBDB)
W 1F08 0 Shift 16 upper bits
R 1014 0 Read last 16 shifted bits (XYZK)

```

Device 2: ODMB JTAG

“Y” refers to the number of bits to be shifted

| Instruction | Description |
|---------------|---|
| W 2Y00 | Shift Data; no TMS header; no TMS tailer |
| W 2Y04 | Shift Data with TMS header only |
| W 2Y08 | Shift Data with TMS tailer only |
| W 2Y0C | Shift Data with TMS header & TMS tailer |
| | |
| R 2014 | Read TDO register |
| | |
| W 2018 | Resets JTAG protocol to IDLE state (data sent with this command is disregarded) |
| | |
| W 2Y1C | Shift Instruction register |
| | |
| W 2020 | Change polarity of V6_JTAG_SEL |

Example: Read ODMB UserCode

Read FPGA UserCode:

```

W 291c 3C8 Set instruction register to 3C8 (read UserCode)
W 2F04 0 Shift 16 lower bits
R 2014 0 Read last 16 shifted bits (DBDB)
W 2F08 0 Shift 16 upper bits
R 2014 0 Read last 16 shifted bits (XYZK)

```

Device 3: ODMB/DCFEB control

| Instruction | Description |
|-----------------|--|
| W/R 3000 | ODMB_CTRL register |
| W/R 3010 | DCFEB_CTRL register |
| | |
| W/R 3020 | TP_SEL register (selects which signals are sent to TP27, TP28, TP41, TP42) |
| | |
| W/R 3100 | LOOPBACK: 0 → no loopback, 1 or 2 → internal loopback |
| W/R 3110 | DIFFCTRL (TX voltage swing): 0 → minimum ~100 mV, F → maximum ~1100mV |
| R 3120 | Read DONE bits from DCFEBs (7 bits) |
| | |
| R 3YZC | Read ODMB_DATA corresponding to selection YZ (see below) |

Bit specification of ODMB_CTRL and DCFEB_CTRL

- ODMB_CTRL[3:0] - Selects CAL_TRGEN (calibration mode).
- ODMB_CTRL[4] - Selects CAL_MODE (calibration mode).
- ODMB_CTRL[5] - Selects CAL_TRGSEL (calibration mode).
- ODMB_CTRL[7] - Selects DCFEB data path: 0 → real data, 1 → dummy data.
- **ODMB_CTRL[8] - Resets FPGA registers/FIFOs and LEDs 1-12 blink for ~3s. Bit is auto-reset.**
- ODMB_CTRL[9] - Selects L1A and LCTs: 0 → from CCB, 1 → internally generated.
- ODMB_CTRL[10] - Selects LVMB: 0 → real LVMB, 1 → dummy LVMB.
- ODMB_CTRL[11] - Kills L1A.
- ODMB_CTRL[12] - Kills L1A_MATCH.
- ODMB_CTRL[13] - 0 → normal, 1 → pedestal (L1A_MATCHes sent to DCFEBs for each L1A).
- ODMB_CTRL[14] - 0 → normal, 1 → pedestal (OTMB data requested for each L1A, needs spec. OTMB FW).
- **DCFEB_CTRL[0] - Reprograms the DCFEBs. Bit is auto-reset.**
- DCFEB_CTRL[1] - Resynchronizes the L1A_COUNTER of ODMB and DCFEBs. Bit is auto-reset.
- DCFEB_CTRL[2] - Sends INJPLS signal to DCFEBs. Bit is auto-reset.
- DCFEB_CTRL[3] - Sends EXTPLS signal to DCFEBs. Bit is auto-reset.
- DCFEB_CTRL[4] - Sends test L1A and L1A_MATCH to all DCFEBs. Bit is auto-reset.
- DCFEB_CTRL[5] - Sends LCT request to OTMB. Bit is auto-reset.
- DCFEB_CTRL[6] - Sends external trigger request to OTMB. Bit is auto-reset.
- DCFEB_CTRL[7] - Resets the optical transceivers. Bit is auto-reset.

Information accessible via command "R 3YZC"

- ▶ YZ = 3F: Least significant 16 bits of L1A_COUNTER
- ▶ YZ = 21-29: Number of L1A_MATCHes for given DCFEB, OTMB, ALCT
- ▶ YZ = 31-37: Gap (in number of bunch crossings) between the last LCT and L1A for given DCFEB
- ▶ YZ = 38: Gap (in number of bunch crossings) between the last L1A and OTMBDAV
- ▶ YZ = 39: Gap (in number of bunch crossings) between the last L1A and ALCTDAV
- ▶ YZ = 41-49: Number of packets stored for given DCFEB, TMB, or ALCT
- ▶ YZ = 4A: Number of packets sent to the DDU
- ▶ YZ = 4B: Number of packets sent to the PC
- ▶ YZ = 51-59: Number of packets shipped to DDU and PC for given DCFEB, TMB, or ALCT
- ▶ YZ = 61-67: Number of data packets received with good CRC for given DCFEB
- ▶ YZ = 71-77: Number of LCTs for given DCFEB
- ▶ YZ = 78: Number of available OTMB packets
- ▶ YZ = 79: Number of available ALCT packets

- ▶ YZ = 5A: Read last CCB_CMD[5:0] + EVTRST + BXRST strobed
- ▶ YZ = 5B: Read last CCB_DATA[7:0] strobed
- ▶ YZ = 5C: Read toggled CCB_CAL[2:0] + CCB_BX0 + CCB_BXRST + CCB_L1ARST + CCB_L1A + CCB_CLKEN + CCB_EVTRST + CCB_CMD_STROBE + CCB_DATA_STROBE
- ▶ YZ = 5D: Read toggled CCB_RSV signals

Device 4: Configuration registers

| Instruction | Description |
|-----------------|---|
| W/R 4000 | LCT_L1A_DLY[5:0] → Set to LCT/L1A gap - 100 |
| W/R 4004 | OTMB_DLY[4:0] → Set to L1A/OTMBDAV gap - 1 |
| W/R 4008 | PUSH_DLY[4:0] |
| W/R 400C | ALCT_DLY[4:0] → Set to L1A/ALCTDAV gap - 1 |
| W/R 4010 | INJ_DLY[4:0] - Delay: 12.5*INJ_DLY [ns] |
| W/R 4014 | EXT_DLY[4:0] - Delay: 12.5*EXT_DLY [ns] |
| W/R 4018 | CALLCT_DLY[3:0] - Delay: 25*CALLCT_DLY [ns] |
| W/R 401C | KILL[9:1] (ALCT + TMB + 7 DCFEBs) |
| W/R 4020 | CRATEID[6:0] |
| W/R 4028 | Number of words generated by dummy DCFEBs, OTMB, and ALCT |
| | |
| R 4100 | Read ODMB unique ID |
| R 4200 | Read firmware version |
| R 4300 | Read firmware build |
| R 4400 | Read month/day firmware was synthesized |
| R 4500 | Read year firmware was synthesized |

Notes

1. If unique ID not set, request UCSB to write it.

Device 5: Test FIFOs

Z refers to FIFO: 1 → PC TX, 2 → PC RX, 3 → DDU TX, 4 → DDU RX, 5 → OTMB, 6 → ALCT

| Instruction | Description |
|-----------------|--|
| R 5000 | Read one word of selected DCFEB FIFO |
| R 500C | Read numbers of words stored in selected DCFEB FIFO |
| W/R 5010 | Select DCFEB FIFO |
| W 5020 | Reset DCFEB FIFOs (7 bits, one per FIFO, which are auto-reset) |
| | |
| R 5Z00 | Read one word of FIFO |
| R 5Z0C | Read numbers of words stored in FIFO |
| W 5Z20 | Reset FIFO |

Notes

- All these FIFOs can hold a maximum of 2,000 18-bit words (36 kb)
- The **OTMB**, **ALCT**, and **7 DCFEB FIFOs** store the data as it arrives in parallel to the standard data path
 - They can hold a maximum of 3 OTMB, 4 ALCT, and 2 DCFEB data packets
- The **DDU TX FIFO** stores DDU packets just before being transmitted
 - They include the DDU header (4 words starting with 9, 4 starting with A), ALCT data, TMB data, DCFEB data, and trailer (4 words starting with F, 4 starting with E)
- The **PC TX FIFO** stores DDU packets wrapped in ethernet frames just before being transmitted
 - They include the ethernet header (4 words) and trailer (4 words)
 - They need to be at least 32 words long
- The **DDU** and **PC RX FIFOs** can be used for loopback tests

Device 6: BPI Interface (PROM)

Important: Instruction 6000 takes ~1 second, during which Device 4 and 6 write commands are ignored

| Instruction | Description |
|---------------|---|
| W 6000 | Write configuration registers to PROM |
| W 6004 | Set configuration registers to retrieved values from PROM |
| | |
| W 6020 | Reset BPI interface state machines |
| W 6024 | Disable parsing commands in command FIFO while filling FIFO with commands (no data) |
| W 6028 | Enable parsing commands in the command FIFO (no data) |
| W 602C | Write one word to command FIFO |
| | |
| R 6030 | Read one word from read-back FIFO |
| R 6034 | Read number of words in read-back FIFO |
| R 6038 | Read BPI Interface Status Register |
| | |
| R 603C | Read Timer (16 LSBs) |
| R 6040 | Read Timer (16 MSBs) |

Device 7: ODMB monitoring

Reads output of the ADC inside the FPGA

| Instruction | Description |
|-------------|---|
| R 7000 | FPGA temperature |
| R 7100 | LV_P3V3: input to FPGA regulators |
| R 7110 | P5V: input to PPIB regulator and level for 5V chips |
| R 7120 | THERM2: board temperature at the center-top |
| R 7130 | P3V3_PP: voltage level for PPIB |
| R 7140 | P2V5: voltage level for FPGA and 2.5V chips |
| R 7150 | THERM1: board temperature close to the LVMB connector |
| R 7160 | P1V0: voltage level for FPGA |
| R 7170 | P5V_LVMB: voltage level for LVMB |

Translation into temperatures and voltages

The output of the 7YZ0 commands is a 12-bit number that we call R_{YZ} . The measurement is:

- The FPGA temperature is $T_{\text{FPGA}} = \frac{R_{00} \times 503.975}{4096} - 273.15$ [$^{\circ}\text{C}$]
- The temperature of the thermistors THERM1, THERM2 is given by

| | | | | | | | | | | |
|----------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| R_{XY} | 377 | 455 | 55A | 687 | 7DD | 959 | AF8 | CB5 | E87 | FFF |
| T [$^{\circ}\text{C}$] | 15 | 20 | 25 | 30 | 35 | 40 | 45 | 50 | 55 | 60 |

- The voltage levels are $V_{YZ} = \frac{R_{YZ}}{2048} \times V_{YZ, \text{Nom}}$ [V], where $V_{YZ, \text{Nom}}$ is the nominal voltage level for that register. That is, $V_{10, \text{Nom}} = V_{13, \text{Nom}} = 3.3\text{V}$, $V_{11, \text{Nom}} = V_{17, \text{Nom}} = 5\text{V}$, $V_{14, \text{Nom}} = 2.5\text{V}$, and $V_{16, \text{Nom}} = 1\text{V}$.

Device 8: Low voltage monitoring

| Instruction | Description |
|---------------|---|
| W 8000 | Send control byte to ADC |
| R 8004 | Read ADC |
| | |
| W 8010 | Select DCFEBs/ALCT to be powered on (8 bits, ALCT + 7 DCFEBs) |
| R 8018 | Read which DCFEBs/ALCT are powered on |
| | |
| W 8020 | Select ADC to be read, 0 to 6 |
| R 8024 | Read which ADC is to be read |

Table 1. Control-Byte Format

| BIT 7 (MSB) | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 (LSB) |
|-------------|-------|-------|-------|-------|-------|-------|-------------|
| START | SEL2 | SEL1 | SEL0 | RNG | BIP | PD1 | PD0 |

| PD1 | PD0 | MODE |
|-----|-----|--|
| 0 | 0 | Normal operation (always on), internal clock mode. |
| 0 | 1 | Normal operation (always on), external clock mode. |
| 1 | 0 | Standby power-down mode (STBYPD), clock mode unaffected. |
| 1 | 1 | Full power-down mode (FULLPD), clock mode unaffected. |

| INPUT RANGE | RNG | BIP |
|-------------|-----|-----|
| 0 to +5V | 0 | 0 |
| 0 to +10V | 1 | 0 |
| ±5V | 0 | 1 |
| ±10V | 1 | 1 |

Device 9: System tests

| Instruction | Description |
|-----------------|--|
| W 9000 | Test the DDU TX/RX with a given number of PRBS 2^7-1 sequences |
| R 900C | Read number of errors during last DDU PRBS test |
| | |
| W 9100 | Test the PC TX/RX with a given number of PRBS 2^7-1 sequences |
| R 910C | Read number of errors during last PC PRBS test |
| | |
| W 9200 | Check N*10000 bits from the PRBS pattern sent by the DCFEB |
| W/R 9204 | Select DCFEB fiber to perform PRBS test |
| R 9208 | Read number of error edges during last DCFEB PRBS test |
| R 920C | Read number of bit errors during last DCFEB PRBS test |
| W/R 9300 | Set PRBS type for DCFEB: 1 → PRBS-7, 2 → PRBS-15, 3 → PRBS-23, 4 → PRBS-31 |
| | |
| W 9400 | Check N*10000 bits from the PRBS pattern sent by the OTMB |
| R 9404 | Read number of enables sent by the OTMB |
| R 9408 | Read number of good 10000 bits sent by the OTMB |
| R 940C | Read number of bit errors during last OTMB PRBS test |
| W 9410 | Reset number of errors in OTMB counter |

Firmware block diagram

The firmware can be downloaded from http://github.com/odmb/odmb_ucsb_v2

