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ODMB user's manual

Optical DAQ MotherBoard for the ME1/1 stations of the CMS muon endcap detector

Firmware tag: V00-03

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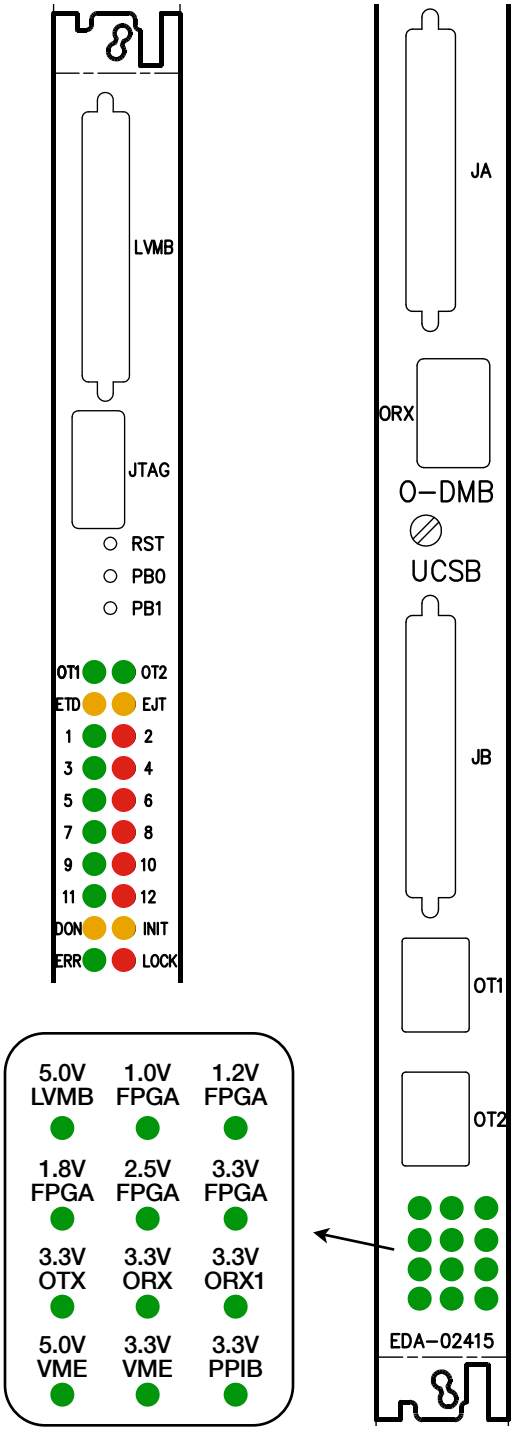
Front panel



Push buttons

- **RST**: Reloads firmware in PROM onto FPGA
- **PB0**: Resets registers/FIFOs in FW. **LEDs 1-12** blink at different speeds for ~3s
- **PB1**: Sends L1A and L1A_MATCH to all DCFEBs. Turns on **LED 12**

LEDs set in firmware

- **1**: 4 Hz signal from clock for data → DDU
- **3**: 2 Hz signal from clock for data → PC
- **5**: 1 Hz signal from internal ODMB clock
- **7**: Internal PLL is locked
- **9**: L1A and LCTs from CCB are selected
- **11**: Path for real DCFEB data is selected
- **2**: Bit 0 of L1A_COUNTER
- **4**: Bit 1 of L1A_COUNTER
- **6**: Bit 2 of L1A_COUNTER
- **8**: Bit 3 of L1A_COUNTER
- **10**: Bit 4 of L1A_COUNTER
- **12**: Briefly ON when a VME command is received. Also ON when **PB1** is pressed

LEDs set in hardware

- **OT1**: SD signal from OT1
- **OT2**: SD signal from OT2
- **ETD**: DTACK enable for discrete logic (logic low)
- **EJD**: JTAG enable for discrete logic (logic low)
- **DON**: DONE signal from FPGA. ON when programmed
- **INIT**: INIT_B signal from FPGA (logic low)
- **ERR**: Error on QPLL
- **LOCK**: QPLL is locked
- **Bottom 12**: Voltage monitoring

General

Firmware version

For a given firmware tag **VXY-ZK**:

- Usercode is **XYZKdbdb**
- FW_VERSION read via "`R 4424`" is **XYZK**

VME access through the board discrete "emergency" logic

The FPGA may be accessed via JTAG through the discrete logic as follows

- The VME address is 0xFFFC
- The bit 0 of the data sent is TMS
- The bit 1 of the data sent is TDI

For example, to read the Usercode, starting from JTAG idle (five TMS = 1 & one TMS = 0), the commands are:

```
W  FFFC  1   To Select-DR-Scan
W  FFFC  1   To Select-IR-Scan
W  FFFC  0   To Capture-IR
W  FFFC  0   To Shift-IR

W  FFFC  0   Shifting IR (Read UserCode IR = 3C8)
W  FFFC  0   Shifting IR
W  FFFC  0   Shifting IR
W  FFFC  2   Shifting IR
W  FFFC  0   Shifting IR
W  FFFC  0   Shifting IR
W  FFFC  2   Shifting IR
W  FFFC  2   Shifting IR
W  FFFC  2   Shifting IR
W  FFFC  3   Shifting IR and to Exit1-IR

W  FFFC  1   To Update-IR
W  FFFC  0   To Run_Test/Idle
W  FFFC  1   To Select-DR-Scan
W  FFFC  0   To Capture-DR

W  FFFC  0   Shifting DR
R  FFFC  0   Shifting DR (Read bit 0 of UserCode)
```

Since the Usercode register is 32 bits, the last two commands should be repeated 31 more times.

Device 1: DCFEB JTAG

"Y" refers to the number of bits to be shifted

Instruction	Description
W 1Y00	Shift Data; no TMS header; no TMS tailer
W 1Y04	Shift Data with TMS header only
W 1Y08	Shift Data with TMS tailer only
W 1Y0C	Shift Data with TMS header & TMS tailer
R 1Y14	Read TDO register
W 1018	Resets JTAG protocol to IDLE state (data sent with this command is disregarded)
W 1Y1C	Shift Instruction register
W 1020	Select DCFEB, one bit per DCFEB
R 1024	Read which DCFEB is selected

Example: Read DCFEB UserCode

DCFEB registers are set and read via JTAG. The following procedure reads the 32-bit USERID of DCFEB 3:

1. Select the appropriate DCFEB setting a 7 bit register, one bit per DCFEB
   - `W 1020 4 ==> Selects DCFEB 3`
2. Set the instruction register to read USERID
   - `W 191C 3C8 ==> This instruction is hardcoded in DCFEB`
3. Shift data and read result
   - `W 1F04 0 ==> First 16 bits with only TMS header`
   - `R 1F14`
   - `W 1F08 0 ==> Finish with only TMS tail`
   - `R 1F14`

Device 2: ODMB JTAG

"Y" refers to the number of bits to be shifted

Instruction	Description
W 2Y00	Shift Data; no TMS header; no TMS tailer
W 2Y04	Shift Data with TMS header only
W 2Y08	Shift Data with TMS tailer only
W 2Y0C	Shift Data with TMS header & TMS tailer
R 2Y14	Read TDO register
W 2018	Resets JTAG protocol to IDLE state (data sent with this command is disregarded)
W 2Y1C	Shift Instruction register
W 2020	Set V6_JTAG_SEL: 0 → discrete logic JTAG, 1 → ODMB JTAG
R 2024	Read V6_JTAG_SEL

Example: Read ODMB UserCode

Read FPGA UserCode:

```
W  2020    1     Set V6_JTAG_SEL to 1 (ODMB JTAG)
W  291c  3C8     Set instruction register to 3C8 (read UserCode)
W  2F04    0     Shift 16 lower bits
R  2F14    0     Read last 16 shifted bits (DBDB)
W  2F14    0     Shift 16 upper bits
R  2F14    0     Read last 16 shifted bits (XYZK)

W  2020    0     Set V6_JTAG_SEL back to 0 (discrete logic JTAG)
```

Device 3: ODMB/DCFEB control

Instruction	Description
W 3000	Set ODMB_CTRL register
R 3004	Read ODMB_CTRL register
W 3010	Set DCFEB_CTRL register
R 3014	Read DCFEB_CTRL register
W 3020	Set TP_SEL register (selects which signals are sent to TP27, TP28, TP41, TP42)
R 3024	Read TP_SEL register
W 3100	Set LOOPBACK: 0 → no loopback, 1 or 2 → internal loopback
R 3104	Read LOOPBACK
W 3110	Set DIFFCTRL (TX voltage swing): 0 → minimum ~100 mV, F → maximum ~1100mV
R 3114	Read DIFFCTRL
R 3YZC	Read ODMB_DATA corresponding to selection **YZ** (see below)

Bit specification of ODMB_CTRL and DCFEB_CTRL

- ODMB_CTRL[3:0] - Selects CAL_TRGEN (calibration mode).
- ODMB_CTRL[4] - Selects CAL_MODE (calibration mode).
- ODMB_CTRL[5] - Selects CAL_TRGSEL (calibration mode).
- ODMB_CTRL[7] - Selects DCFEB data path: 0 → real data, 1 → dummy data.
- **ODMB_CTRL[8] - Resets FPGA registers/FIFOs and LEDs 1-12 blink for ~3s. Bit is auto-reset.**
- ODMB_CTRL[9] - Selects L1A and LCTs: 0 → from CCB, 1 → internally generated.
- ODMB_CTRL[10] - Selects LVMB: 0 → real LVMB, 1 → dummy LVMB.
- ODMB_CTRL[11] - Kills L1A.
- ODMB_CTRL[12] - Kills L1A_MATCH.

- **DCFEB_CTRL[0] - Reprograms the DCFEBs. Bit is auto-reset.**
- DCFEB_CTRL[1] - Resynchronizes the L1A_COUNTER of ODMB and DCFEBs. Bit is auto-reset.
- DCFEB_CTRL[2] - Sends INJPLS signal to DCFEBs. Bit is auto-reset.
- DCFEB_CTRL[3] - Sends EXTPLS signal to DCFEBs. Bit is auto-reset.
- DCFEB_CTRL[4] - Sends test L1A and L1A_MATCH to all DCFEBs. Bit is auto-reset.
- DCFEB_CTRL[15:10] - Selects FSEL.

Information accessible via command "R 3YZC"

- YZ = 3A: Most significant 8 bits of L1A_COUNTER
- YZ = 3B: Least significant 16 bits of L1A_COUNTER
- YZ = 21-27: Number of L1A_MATCH for given DCFEB
- YZ = 31-37: Gap (in number of bunch crossings) between the last LCT and L1A for given DCFEB
- YZ = 41-49: Number of packets stored for given DCFEB, TMB, or ALCT
- YZ = 51-59: Number of packets shipped to DDU and PC for given DCFEB, TMB, or ALCT
- YZ = 61-67: Number of data packets received with good CRC for given DCFEB

Device 4: Configuration registers

Instruction	Description
W 4000	Set LCT_L1A_DLY[5:0] - Total delay: 2400 + 25*DCT_L1A_DLY [ns]
W 4004	Set TMB_DLY[4:0]
W 4008	Set PUSH_DLY[4:0]
W 400C	Set ALCT_DLY[4:0]
W 4010	Set INJ_DLY[4:0] - Delay: 12.5*INJ_DLY [ns]
W 4014	Set EXT_DLY[4:0] - Delay: 12.5*EXT_DLY [ns]
W 4018	Set CALLCT_DLY[3:0] - Delay: 25*CALLCT_DLY [ns]
W 401C	Set KILL[9:1] (ALCT + TMB + 7 DCFEBs)
W 4020	Set CRATEID[6:0]
R 4400	Read LCT_L1A_DLY
R 4404	Read TMB_DLY
R 4408	Read PUSH_DLY
R 440C	Read ALCT_DLY
R 4410	Read INJ_DLY
R 4414	Read EXT_DLY
R 4418	Read CALLCT_DLY
R 441C	Read KILL
R 4420	Read CRATEID
R 4424	Read FW_VERSION

Device 5: Test FIFOs

Z refers to FIFO: 1 → PC TX, 2 → PC RX, 3 → DDU TX, 4 → DDU RX

Instruction	Description
R 5000	Read one word of selected DCFEB FIFO
R 500C	Read numbers of words stored in selected DCFEB FIFO
W 5010	Select DCFEB FIFO
R 5014	Read which DCFEB FIFO is selected
W 5020	Reset DCFEB FIFOs (7 bits, one per FIFO, which are auto-reset)
R 5Z00	Read one word of FIFO
R 5Z0C	Read numbers of words stored in FIFO
W 5Z20	Reset FIFO

Notes

1. All these FIFOs can hold a maximum of 2,250 words (36 kb)
2. The **7 DCFEB FIFOs** store the DCFEB data as it arrives in parallel to the standard data path
   - They can hold a maximum of 2 data packets
3. The **DDU TX FIFO** stores DDU packets just before being transmitted
   - They include the DDU header (4 words starting with 9, 4 starting with A), ALCT data, TMB data, DCFEB data, and trailer (4 words starting with F, 4 starting with E)
4. The **PC TX FIFO** stores DDU packets wrapped in ethernet frames just before being transmitted
   - They include the ethernet header (4 words) and trailer (4 words)
   - They need to be at least 32 words long
5. The **DDU** and **PC RX FIFOs** can be used for loopback tests

Device 8: Low voltage monitoring

Instruction	Description
W 8000	Send control byte to ADC
R 8004	Read ADC
W 8010	Select DCFEBs/ALCT to be powered on (8 bits, ALCT + 7 DCFEBs)
R 8014	Read which DCFEBs/ALCT are powered on
W 8020	Select ADC to be read
R 8024	Read which ADC is to be read