



11<sup>th</sup> June 2013

# ODMB user's manual

Optical DAQ MotherBoard for the ME1/1 stations of the CMS muon endcap detector

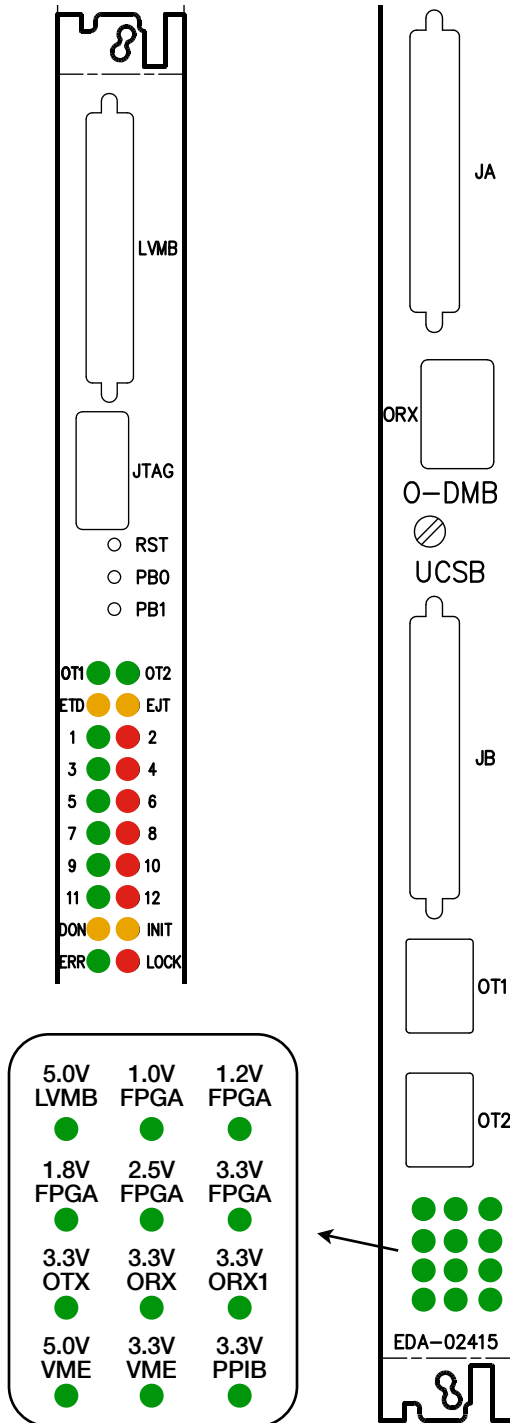
Firmware tag: V00-02

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# Front panel



## Push buttons

- **RST**: Reloads firmware in PROM onto FPGA
- **PB0**: Resets registers/FIFOs in FW. **LEDs 1-12** blink at different speeds for ~3s
- **PB1**: Sends L1A and L1A\_MATCH to all DCFEBs. Turns on **LED 12**

## LEDs set in firmware

- **1**: 4 Hz signal from clock used for DCFEB data
- **3**: 2 Hz signal from clock used for DDU data
- **5**: 1 Hz signal from clock used for FPGA
- **7**: Internal PLL is locked
- **9**: L1A and LCTs from CCB are selected
- **11**: Path for real DCFEB data is selected
- **2**: Bit 0 of L1A\_COUNTER
- **4**: Bit 1 of L1A\_COUNTER
- **6**: Bit 2 of L1A\_COUNTER
- **8**: Bit 3 of L1A\_COUNTER
- **10**: Bit 4 of L1A\_COUNTER
- **12**: Briefly ON when a VME command is received. Also ON when **PB1** is pressed

## LEDs set in hardware

- **OT1**: SD signal from OT1
- **OT2**: SD signal from OT2
- **ETD**: DTACK enable for discrete logic (logic low)
- **EJD**: JTAG enable for discrete logic (logic low)
- **DON**: DONE signal from FPGA. ON when programmed
- **INIT**: INIT\_B signal from FPGA (logic low)
- **ERR**: Error on QPLL
- **LOCK**: QPLL is locked
- **Bottom 12**: Voltage monitoring

# General

## Firmware version

For a given firmware tag **VXY-ZK**:

- ❖ Usercode is **XYZKdbdb**
- ❖ FW\_VERSION read via "R 4424" is **XYZK**

## VME access through the board discrete "emergency" logic

The FPGA may be accessed via JTAG through the discrete logic as follows

- ❖ The VME address is 0xFFFC
- ❖ The bit 0 of the data sent is TMS
- ❖ The bit 1 of the data sent is TDI

For example, to read the Usercode, starting from JTAG idle (five TMS = 1 & one TMS = 0), the commands are:

```

W FFFC 1 To Select-DR-Scan
W FFFC 1 To Select-IR-Scan
W FFFC 0 To Capture-IR
W FFFC 0 To Shift-IR

W FFFC 0 Shifting IR (Read UserCode IR = 3C8)
W FFFC 0 Shifting IR
W FFFC 0 Shifting IR
W FFFC 2 Shifting IR
W FFFC 0 Shifting IR
W FFFC 0 Shifting IR
W FFFC 2 Shifting IR
W FFFC 2 Shifting IR
W FFFC 2 Shifting IR
W FFFC 3 Shifting IR and to Exit1-IR

W FFFC 1 To Update-IR
W FFFC 0 To Run_Test/Idle
W FFFC 1 To Select-DR-Scan
W FFFC 0 To Capture-DR

W FFFC 0 Shifting DR
R FFFC 0 Shifting DR (Read bit 0 of UserCode)

```

Since the Usercode register is 32 bits, the last two commands should be repeated 31 more times.

# Device 1: DCFEB JTAG

“Y” refers to the number of bits to be shifted

Instruction	Description
<b>W 1Y00</b>	Shift Data; no TMS header; no TMS tailer
<b>W 1Y04</b>	Shift Data with TMS header only
<b>W 1Y08</b>	Shift Data with TMS tailer only
<b>W 1Y0C</b>	Shift Data with TMS header & TMS tailer
<b>R 1Y14</b>	Read TDO register
<b>W 1018</b>	Resets JTAG protocol to IDLE state (data sent with this command is disregarded)
<b>W 1Y1C</b>	Shift Instruction register
<b>W 1020</b>	Select DCFEB, one bit per DCFEB
<b>R 1024</b>	Read which DCFEB is selected

## Example

DCFEB registers are set and read via JTAG. The following procedure reads the 32-bit USERID of DCFEB 3:

- Select the appropriate DCFEB setting a 7 bit register, one bit per DCFEB
  - W 1020 4 ==> Selects DCFEB 3
- Set the instruction register to read USERID
  - W 191C 3C8 ==> This instruction is hardcoded in DCFEB
- Shift data and read result
  - W 1F04 0 ==> First 16 bits with only TMS header
  - R 1F14
  - W 1F08 0 ==> Finish with only TMS tail
  - R 1F14

# Device 3: ODMB/DCFEB control

Instruction	Description
<b>W 3000</b>	Set ODMB_CTRL register
<b>R 3004</b>	Read ODMB_CTRL register
<b>W 3010</b>	Set DCFEB_CTRL register
<b>R 3014</b>	Read DCFEB_CTRL register
<b>W 3020</b>	Set TP_SEL register (selects which signals are sent to TP27, TP28, TP41, TP42)
<b>R 3024</b>	Read TP_SEL register
<b>R 3YZC</b>	Read ODMB_DATA corresponding to selection <b>YZ</b> (see below)

## Bit specification of ODMB\_CTRL and DCFEB\_CTRL

- ▶ ODMB\_CTRL[3:0] - Selects CAL\_TRGEN (calibration mode).
- ▶ ODMB\_CTRL[4] - Selects CAL\_MODE (calibration mode).
- ▶ ODMB\_CTRL[5] - Selects CAL\_TRGSEL (calibration mode).
- ▶ ODMB\_CTRL[7] - Selects DCFEB data path: 0 real data, 1 dummy data.
- ▶ **ODMB\_CTRL[8] - Resets FPGA registers/FIFOs and LEDs 1-12 blink for ~3s. Bit is auto-reset.**
- ▶ ODMB\_CTRL[9] - Selects L1A and LCTs: 0 from CCB, 1 internally generated.
- ▶ ODMB\_CTRL[10] - Selects LVMB: 0 real LVMB, 1 dummy LVMB.
- ▶ **DCFEB\_CTRL[0] - Reprograms the DCFEBs. Bit is auto-reset.**
- ▶ DCFEB\_CTRL[1] - Resynchronizes the L1A\_COUNTER of ODMB and DCFEBs. Bit is auto-reset.
- ▶ DCFEB\_CTRL[2] - Sends INJPLS signal to DCFEBs. Bit is auto-reset.
- ▶ DCFEB\_CTRL[3] - Sends EXTPLS signal to DCFEBs. Bit is auto-reset.
- ▶ DCFEB\_CTRL[4] - Sends test L1A and L1A\_MATCH to all DCFEBs. Bit is auto-reset.
- ▶ DCFEB\_CTRL[15:10] - Selects FSEL.

## Information accessible via command "R 3YZC"

- ▶ YZ = 21-27: Number of L1A\_MATCH for given DCFEB
- ▶ YZ = 31-37: Gap (in number of bunch crossings) between the last LCT and L1A for given DCFEB
- ▶ YZ = 41-49: Number of packets stored for given DCFEB, TMB, or ALCT
- ▶ YZ = 51-59: Number of packets shipped to DDU and PC for given DCFEB, TMB, or ALCT

# Device 4: Configuration registers

Instruction	Description
<b>W 4000</b>	Set LCT_L1A_DLY[5:0] - Total delay: $2400 + 25 * \text{DCT\_L1A\_DLY}$ [ns]
<b>W 4004</b>	Set TMB_DLY[4:0]
<b>W 4008</b>	Set PUSH_DLY[4:0]
<b>W 400C</b>	Set ALCT_DLY[4:0]
<b>W 4010</b>	Set INJ_DLY[4:0] - Delay: $12.5 * \text{INJ\_DLY}$ [ns]
<b>W 4014</b>	Set EXT_DLY[4:0] - Delay: $12.5 * \text{EXT\_DLY}$ [ns]
<b>W 4018</b>	Set CALLCT_DLY[3:0] - Delay: $25 * \text{CALLCT\_DLY}$ [ns]
<b>W 401C</b>	Set KILL[9:1] (ALCT + TMB + 7 DCFEBs)
<b>W 4020</b>	Set CRATEID[6:0]
<b>R 4400</b>	Read LCT_L1A_DLY
<b>R 4404</b>	Read TMB_DLY
<b>R 4408</b>	Read PUSH_DLY
<b>R 440C</b>	Read ALCT_DLY
<b>R 4410</b>	Read INJ_DLY
<b>R 4414</b>	Read EXT_DLY
<b>R 4418</b>	Read CALLCT_DLY
<b>R 441C</b>	Read KILL
<b>R 4420</b>	Read CRATEID
<b>R 4424</b>	Read FW_VERSION

# Device 5: Test DCFEB FIFOs

**DCFEB data is stored in parallel in these test FIFOs and the FIFOs that ship the data out**

Instruction	Description
<b>R 5000</b>	Read one word of selected FIFO
<b>R 500C</b>	Read numbers of words stored in selected FIFO
<b>W 5010</b>	Select FIFO
<b>R 5014</b>	Read which FIFO is selected
<b>W 5020</b>	Reset FIFOs (7 bits, one per FIFO)



# Device 8: Low voltage monitoring

Instruction	Description
<b>W 8000</b>	Send control byte to ADC
<b>R 8004</b>	Read ADC
<b>W 8010</b>	Select DCFEBs/ALCT to be powered on (8 bits, ALCT + 7 DCFEBs)
<b>R 8014</b>	Read which DCFEBs/ALCT are powered on
<b>W 8020</b>	Select ADC to be read
<b>R 8024</b>	Read which ADC is to be read