Lecture #3:

**ODMB** history and design

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*Richman group meeting*
Outline

1. **ODMB** history
   ✓ Documentation of prototype versions
   ✓ Gives an idea of how a project is carried out

2. **ODMB** design
   ✓ How to read schematics/layout
   ✓ How to find components on board
   ✓ Main hardware blocks

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**Before LS1**
- CSC
  - Wires
  - 42× AFEBS
  - LVDB
  - Strips
  - 5×CFEBs
- ALCT
- TMB
- DMB

**ME1/1 after LS1**
- CSC
  - Wires
  - 42× AFEBS
  - LVDB7
  - Strips
  - 7×DCFEBs
- ALCT-S6
- OTMB
- ODMB

Connections:
- Copper
- Fiber
- Trigger
- DAQ
- UXC
- USC
Motivation for the ODMB

~ ME1/1a was unganged during LS1 (2013-2014)
  ~ 5 CFEBs replaced with 7 DCFEBs

~ New ODMB designed to handle for 7 DCFEBs
  ~ Can save front panel space with optical connections
ODMB.V1 design

Design of the ODMB started in 2010, led by Guido Magazzù at UCSB

Full optical path to DCFEBs both for data and TTC

Optical TTC required design of FF-EMU
- Rad-hard deserializer ASIC
- 1st FF-EMU prototype (May 2011) major problems
- 2nd prototype in March 2012
1st prototype in April 2012

Two snap12 TX for TTC
- 14 fibers to DCFEBs, 10 spares

Two snap12 RX for data
- Also for TTC return

Significant bugs with the clocks patched up with soldered board
ODMB.V1 problems

~ VME communication with ODMB did not work at UCSB
  - Trying to emulate VME crate with FPGA inside computer, connection through a test port
  - Communication did work at B904 test stand at CERN, but needed test stand at UCSB for development

~ 2nd FF-EMU prototype did not work
  - Guido said it was due to the testing procedure, not the chip

~ ODMB fell in critical path of LS1 upgrade
  - No time for more FF-EMU chip submissions
  - Time short for board, firmware, and software development

In December 2012 decided to abandon FF-EMU and switch to copper TTC
ODMB V2 design

- Designed in January 2013 between Guido Magazzù, Ben Bylsma (OSU), Mike Matveev (Rice), Jason Gilmore (Texas A&M), Ray Gerhart (UC Davis)
  - Assisted by Frank Golf and Manuel Franco Sevilla (UCSB) who joined the project in November 2012

- Required a Patch Panel Interconnecting Board (PPIB) to distribute signals to all 7 DCFEBs
  - Designed by Mike Matveev at Rice

Successfully tested ODMB + PPIB + DCFEBs communication.
CFEB-JTAG works.
Exercised basic functionality:
Write/Read registers.
Read UserCode.

Two HD50 connectors to ODMB

Seven HD50 connectors to DCFEBs
Set up an actual lab in early 2013
- Frank and Manuel got trained at Rice
- Borrowed partial VME crate, VCC, LVMB, internet card

With this setup, VME communication worked like at CERN.

Jeff even helped sweeping the floor of the ODMB lab!
Later in 2013, borrowed a full VME crate from Florida
- OSU sent 4 DCFEBs
- Rice sent PPIB
- Northeastern sent skewclear cables

Robust set up for production tests
- Needed to test 90 ODMBs in short period of time

Adam, Alex, Jack, and Tom joined the ODMB team!
Lots of testing and debugging

~ Systematically tested and fixed all functionality and connections
- Bugs were small enough that ODMB.V2 could be patched and show full functionality

Checked linearity of voltage reads from LVMB

\[ V_{\text{meas}} = (0.997 \pm 0.002)V_{\text{ADC}} + (0.006 \pm 0.012) [V] \]

Fixed short with front panel by moving connections farther
Example: problems in optical transmission

~ Optical transmission to DDU some times worked, but there were persistent errors
~ Measured low voltage swing on inputs to transceivers → FPGA not generating enough swing
~ After poring over the documentation, found we were missing 100 Ω resistor and 1.2V connection!

Loopback test to check data transmission to DDU
(uses RX/TX in Finisar transceivers and FPGA)
Received 5 boards on Apr 2013
- 12 input fibers for DCFEB data
- Two bidirectional HD50 connectors for DCFEB TTC, PPIB power

Showed full functionality with \textit{ODMB}.V2
- Fixed JTAG to DCFEBs
- Fixed JTAG to ODMB
- Fixed opt. TX (missing resistor/voltage)
- Moved connector to avoid short

Passed Production Readiness Review (PRR) on Oct 2013
- Proceeded with pre-production of 10 \textit{ODMB}.V3 boards
Production tests

~ Developed software and firmware to systematically test functionality of each board

ODMB Production Tests

DCFEB

Virtex-6 GTX

PRBS generator

Data 8B/10B

With special FW in the DCFEBs/OTMBs, we could stress test inputs to ODMB

ODMB

Virtex-6 GTX

PRBS checker

10B/8B Data

ODMB website with all tests

OTMB firmware

ODMB block

VME block

OTMB standard

DMB_RX[5:0]

DMB_TX[48:0]

With special FW in the DCFEBs/OTMBs, we could stress test inputs to ODMB
Final modifications

V3

- CERN store sent wrong part (too tall)
- Removed heat sinks to lower snap-12 profile
- Improved ground/power planes layout, and added thieving

V4

~ The ODMB V3 had full functionality, but made one more design (ODMB V4) to improve robustness and monitoring
- Separation of P1V0 power planes to reduce noise in FPGA optical banks (GTXs or MGTs)
- Addition of capacitors, ground vias
- Addition of PPIB/LVMB current monitoring (fire hazard)
Produced by Pactron in Santa Clara
- 5 pre-production boards on February 2014
- 85 production boards on March-April 2014

Last minute fixes
- Added 22 AWG wire to reduce voltage drop in new P1V0_MGT and bus bar to unconnected vias

All 90 boards tested/fixed in 2 weeks
- 85 boards good, 4 fixed later
- Heroic efforts by Frank, Sicheng, Alex
Installation in May 2014

Adam, Jack, Manuel, and Jeff installed 72 boards into the peripheral crates in CMS in ~4 days.
ODMB hardware
Board development

1. Concept
❖ Ideas in the engineer’s mind
❖ If designer different from engineer, ideas communicated via email and Word documents

2. Schematics
❖ Abstract representation of all connections on the board
❖ Done in Cadence Allegro (ODM), Altium, Kicad, etc.
❖ Look at it in pdf form

3. Layout
❖ Actual geometric representation of all connections on the board
❖ Done in Cadence Allegro (ODM), Altium, Kicad, etc.
❖ Look at it in pdf form

4. PCB fabrication
❖ Fabrication of bare Printed Circuit Board
❖ Uses gerber files produced by design software

5. Assembly
❖ Stuffs components on bare PCBs
❖ Components defined in Bill Of Materials (BOM) in Excel form

Guido, Ben, Mike, Ray, Jason, Manuel for the ODMB
Jean-Marc Combe at CERN for the ODMB
Jean-Marc Combe at CERN for the ODMB
Pactron in Santa Clara for the ODMB
Pactron in Santa Clara for the ODMB
~ 9 page .pdf file

~ Component naming convention
- **IC**: integrated circuit (eg. IC14)
- **J**: connector (eg. J7)
- **R**: resistor (eg. R87)
- **C**: capacitor (eg. C17)
- **L**: inductor (eg. L5)
- **QZ**: quartz oscillator (eg. QZ3)
- **RG**: voltage regulator (eg. RG2)
- **OT/RX**: optical transceiver (eg. OT1)

~ Signal naming convention
- **C**: at the connector (eg. C_VME_ADDR)
- **P**x**y**: voltage level at x.y V (eg. P2V5)
- **_P**: positive LVDS signal (eg. IPPIB_SM_P)
- **_N**: negative LVDS signal (eg. IPPIB_SM_N)
ODMB layout overview

- 20-page .pdf file
- Describes all 12 layers of the board
  - Including ground and power planes
- Mask layer useful to locate components on the board
Backplane VME connector

VME connector (J7) is on page 1

Brings VME_ADDR (instruction) and VME_DATA signals to ODMB
- These define the VME protocol, together with DTACK, WRITE, VME_AM, BG, AS, IACK, ...

Also important VME_GA (geographical address)
- Number that indicates which crate slot the board is plugged into
Voltage level translators

- Level translators (**74ALVC164245DL**) transform digital signals to different voltage level
  - VCCB and VCCA determine the two voltage levels
  - DIR determines the direction of the signals
  - OE is the Output Enable
    * Active low → output enabled if grounded, output is high-impedance (Z) if OE is at VCC

~ Numerous translators throughout the design
Backplane OTMB/CCB connectors

~ OTMB/CCB connectors (J9 and J10) are on pages 2 and 3
  - Right next to each other

~ From CCB, bring CMS 40 MHz clock (CLK_P/N), L1 trigger (L1ACC), BX0, hard reset (CCB_HARDRST_B), calibration (CCB_CAL)

~ From OTMB, bring OTMB data (TMB), ALCT data (ALCT), LCTs (RAWLCT)
DCFEB connector A (J3) is on page 7

- **Carries JTAG signals** that control DCFEBs
  - **TCK**: JTAG clock (to the DCFEBs)
  - **TMS**: mode select (to the DCFEBs)
  - **TDI**: data input (to the DCFEBs)
  - **TDO**: data output (from the DCFEBs)

- Also PPIB power (P3V6_PP), BC0, and some DONE
DCFEB connector B

~ DCFEB connector B (J5) is on page 7
~ Carries clock and triggers to DCFEBs
  - CMSCLK: 40 MHz CMS clock
  - L1A: CMS L1 trigger accept
  - L1A_MATCH_n: coincidence between L1A and LCT
  - INJPLS, EXTPLS: commands for calibration pulses
  - RESYNC: DCFEB reset
  - DONE: DCFEB FPGA ready signal
LVDS ↔ CMOS conversion

- We use two standards
  - **LVDS** (low-voltage differential signaling): voltage swing ~ 700 mV
  - **CMOS/TTL**: single ended with respect to ground

- It is **more robust to send LVDS signals through copper cables**
  - Converters before DCFEB connectors
Optical receivers for DCFEBs

Snap12 optical receiver from DCFEB (RX1) is on page 7
- Uses MTP12 connector
- Only 7 of the 12 signals used in practice

Converts the 3.2 GHz optical signals into copper signals
- Input: light from DCFEBs
- Output: ORX2-nn, 3.2 GHz copper signals that go to the FPGA
Optical transceivers for DDU/PC

Schematics

LEDs showing if fibers connected

Layout

~ Finisar transceivers for DDU/PC (RX1) are on page 7
  - Each transceiver has one TX and one RX
  - Uses LC connector

~ Convert the 1.6/1.25 GHz optical signals into copper signals
  - In normal operation, we only use TX (GL0_TX) to DDU
    * RX could be used to tell the ODMB to stop sending data to DDU because buffers full
  - TX to PC is for debugging, and possibly monitoring
Virtex-6 FPGA (IC33) is on pages 4, 5, and 6

It is the heart of the ODMB

- Handles logic, memory, and high-speed serializers/deserializers for optical transmission
- Also system monitoring (voltages, currents, temperatures)

Main cost driver at ~$800 per FPGA
Virtex-6 FPGA GTX

~ The optical banks of the Virtex-6 FPGA are called GTX
  - Specific implementation of Multi-Gigabit Transceivers (MGT)
  - High-speed signals serialized (16 → 1) or deserialized (1 → 16)
    - ORX2-nn: 12 signals coming from Snap12 RX (DCFEBs) at 3.2 GHz
    - GL0_RX/TX: signal coming from/to Finisar RX/TX (DDU) at 1.6 GHz
    - GL1_RX/TX: signal coming from/to Finisar RX/TX (PC) at 1.25 GHz

~ Clocks can only be distributed one bank over
  - eg. GL0_CLK on bank 113 can only reach banks 112, 113, and 114

80/125 MHz oscillators for DDU/PC transmission