



# Optical Loop Back Test for ODMB7 Preproduction

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## Basic idea

- All TX ports sending PRBS signals
- All RX ports verify for errors
- Does not have to be 1-1 with TX ports

- Data flow:
  - FPGA → B04 → B04 → FPGA (4 lines)
  - Multiplier (12×) → T12 → R12 → FPGA (1 line)
  - FPGA → Finisar → Finisar → FPAG (1 line)

- All related pins are added to constraint file

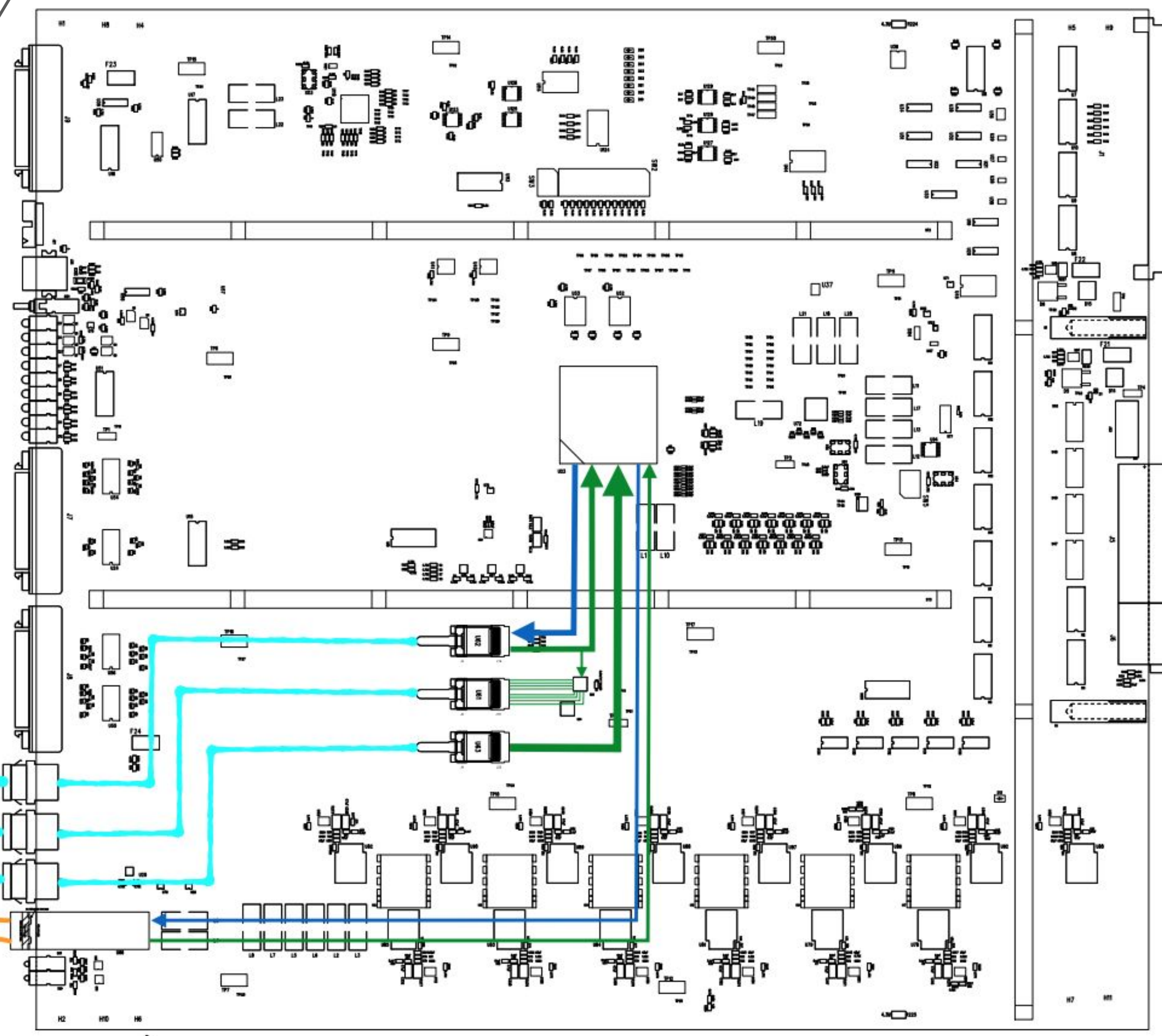
B04: 4 in, 4 out

T12: 12 out

R12: 12 in

Finisar: 1 in, 1 out

Simple counting gives 17 tx and 17 rx, but not all of them go into the FPGA



This test relies on PRBS generator and checker inside the FPGA (GTH transceiver)

16 PRBS generators/checkers in this version

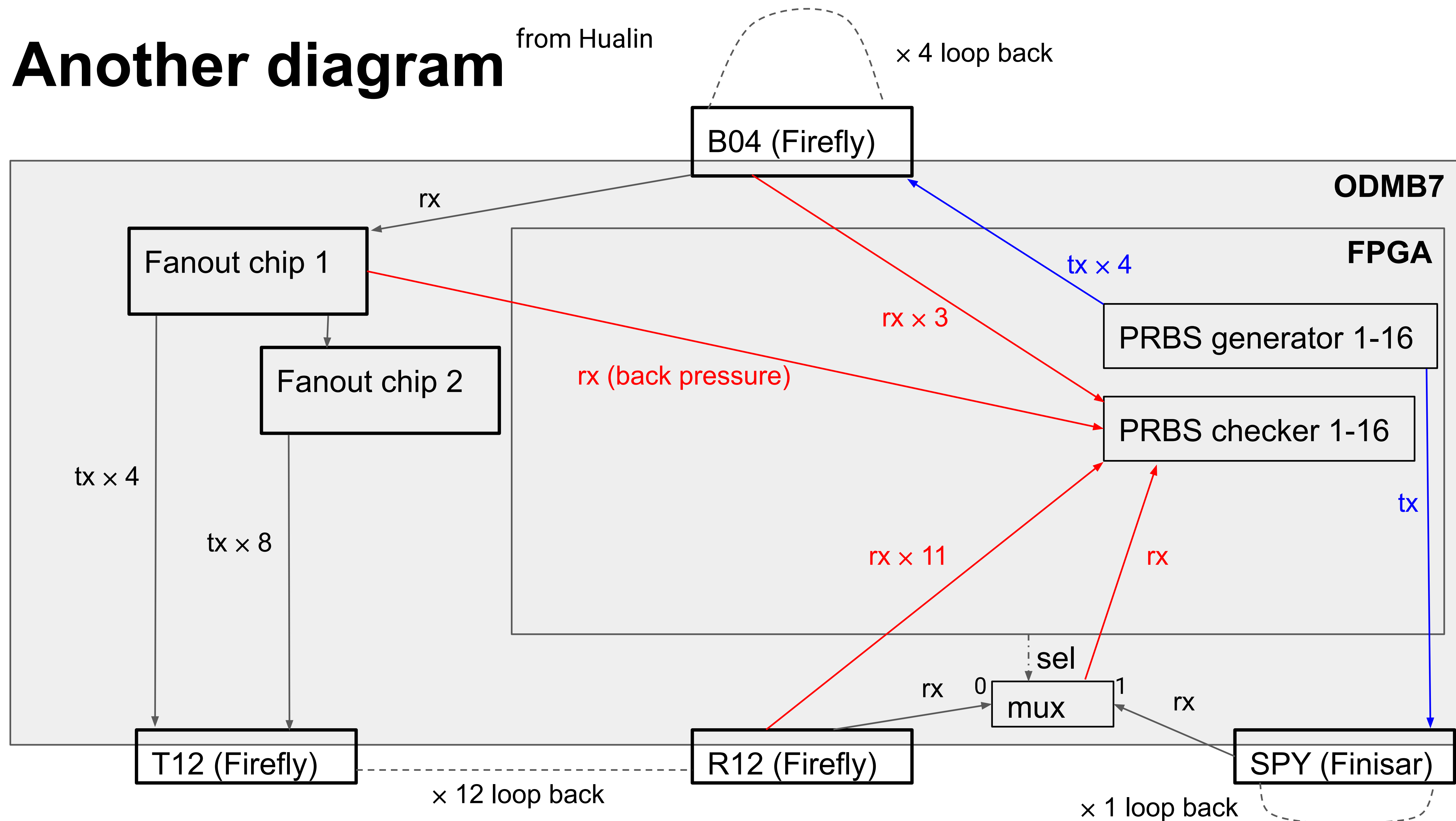
Firmware compatible with ODMB7 is here:

[https://github.com/wsicheng/ODMBDevelopment/tree/master/SingleTestFWs/optical\\_ibert\\_gth](https://github.com/wsicheng/ODMBDevelopment/tree/master/SingleTestFWs/optical_ibert_gth)



## Another diagram

from Hualin







## ❖ Step 1: Preparation

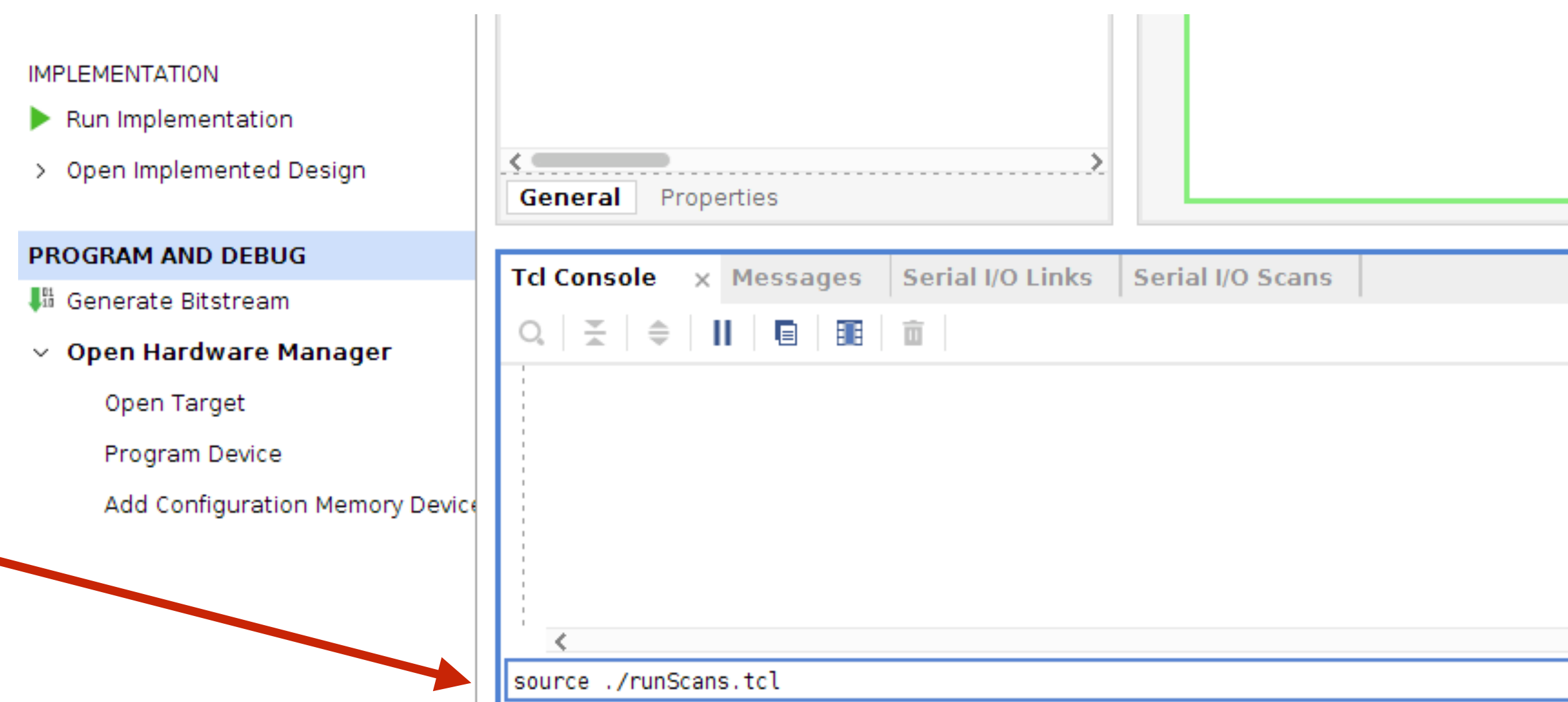
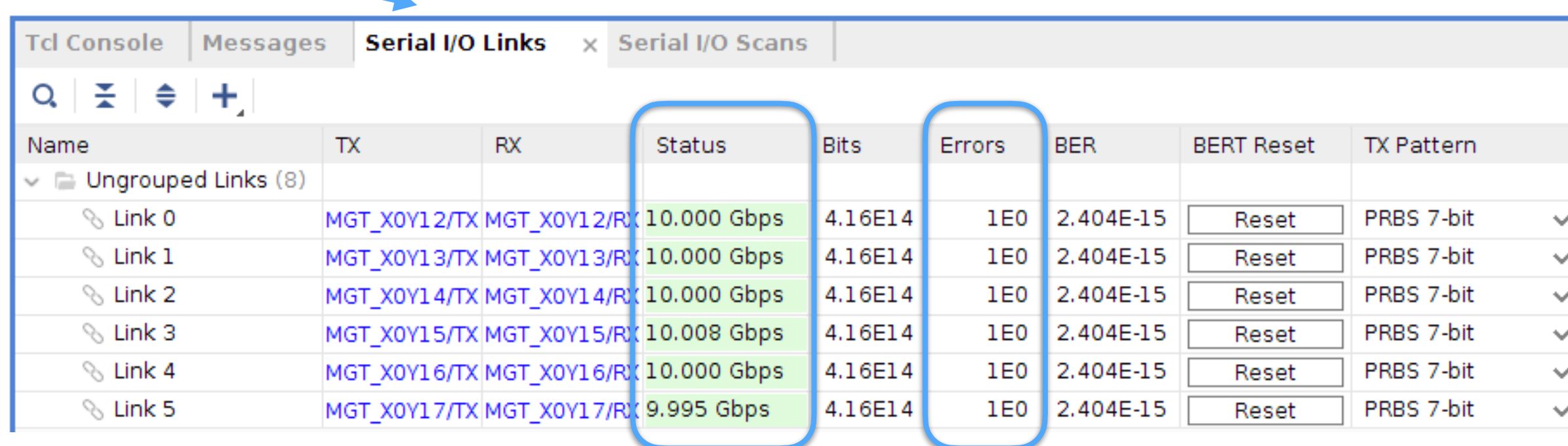
- Connect to board and load firmware \*
- Edit the constants at the top of runScans.tcl

## ❖ Step 2: Run script from the Tcl console \*

- source runScans.tcl

## ❖ Step 3: Evaluate results from “Serial I/O Links”

- Verify that the Link status are good
- Verify that the Error count is stable at one
- Look at the IBERT scans plots (next slide)

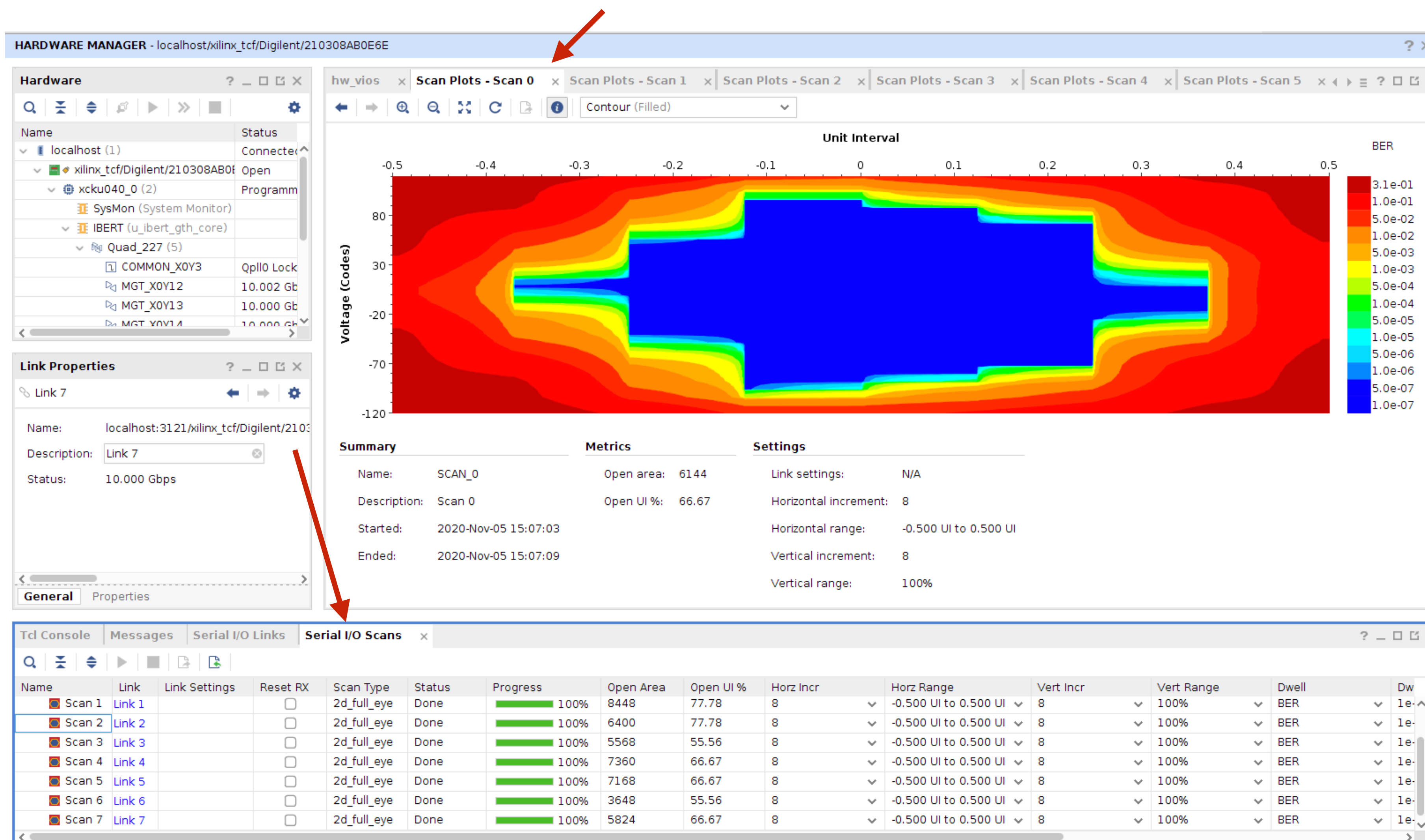
Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern
Ungrouped Links (8)								
Link 0	MGT_X0Y12/TX	MGT_X0Y12/RX	10.000 Gbps	4.16E14	1E0	2.404E-15	Reset	PRBS 7-bit
Link 1	MGT_X0Y13/TX	MGT_X0Y13/RX	10.000 Gbps	4.16E14	1E0	2.404E-15	Reset	PRBS 7-bit
Link 2	MGT_X0Y14/TX	MGT_X0Y14/RX	10.000 Gbps	4.16E14	1E0	2.404E-15	Reset	PRBS 7-bit
Link 3	MGT_X0Y15/TX	MGT_X0Y15/RX	10.008 Gbps	4.16E14	1E0	2.404E-15	Reset	PRBS 7-bit
Link 4	MGT_X0Y16/TX	MGT_X0Y16/RX	10.000 Gbps	4.16E14	1E0	2.404E-15	Reset	PRBS 7-bit
Link 5	MGT_X0Y17/TX	MGT_X0Y17/RX	9.995 Gbps	4.16E14	1E0	2.404E-15	Reset	PRBS 7-bit

\* Firmware and the automated script can be found at:

[http://hep.ucsb.edu/cms/odmb\\_noCVS/firmware/odmb7/preproduction/optical\\_loopback\\_ibert/](http://hep.ucsb.edu/cms/odmb_noCVS/firmware/odmb7/preproduction/optical_loopback_ibert/)

- ▶ The scans will pop up one by one during the script running
- ▶ The Open area should be the main indicator on link quality

Running eye scan will create errors to the link, so it's normal to see error count increase during running of the eye scan, and the link shall be reset afterward



## ❖ Configurable constants

- FPGA name
- The PRBS pattern sent and checked by TX/RX
- Auto load firmware with the script (need to specify filename)
- Disable the SPY\_TX\_P/N channels
  - Set to 1 for the 12.48 Gb/s version, 0 for the 4.0 Gb/s version
- Tag: suffix to the log file

## ❖ Steps performed by the script

- Make a link between each available txs and rxes
- Reset all good links and inject 1 error
- Config and run Eye Scans on each good link
  - The **open area**, **open percentage**, **horizontal percentage** and **vertical percentage** will be written to a log file
- Reset again and inject 1 error
- Loop to fetch the BER values in certain time period
  - Write **total bits received**, **error count**, **bit error rate (BER)**, **RX pattern** each turn into file for later plotting/analysis

```

8  set DEVICE_NAME {xcku040_0}
9  set PRBS_PATTERN {PRBS 31-bit}

17 set programfpga 0
18 set bitfilename {}
19 set disable_spy_tx 0
20 set tag "test2"

```