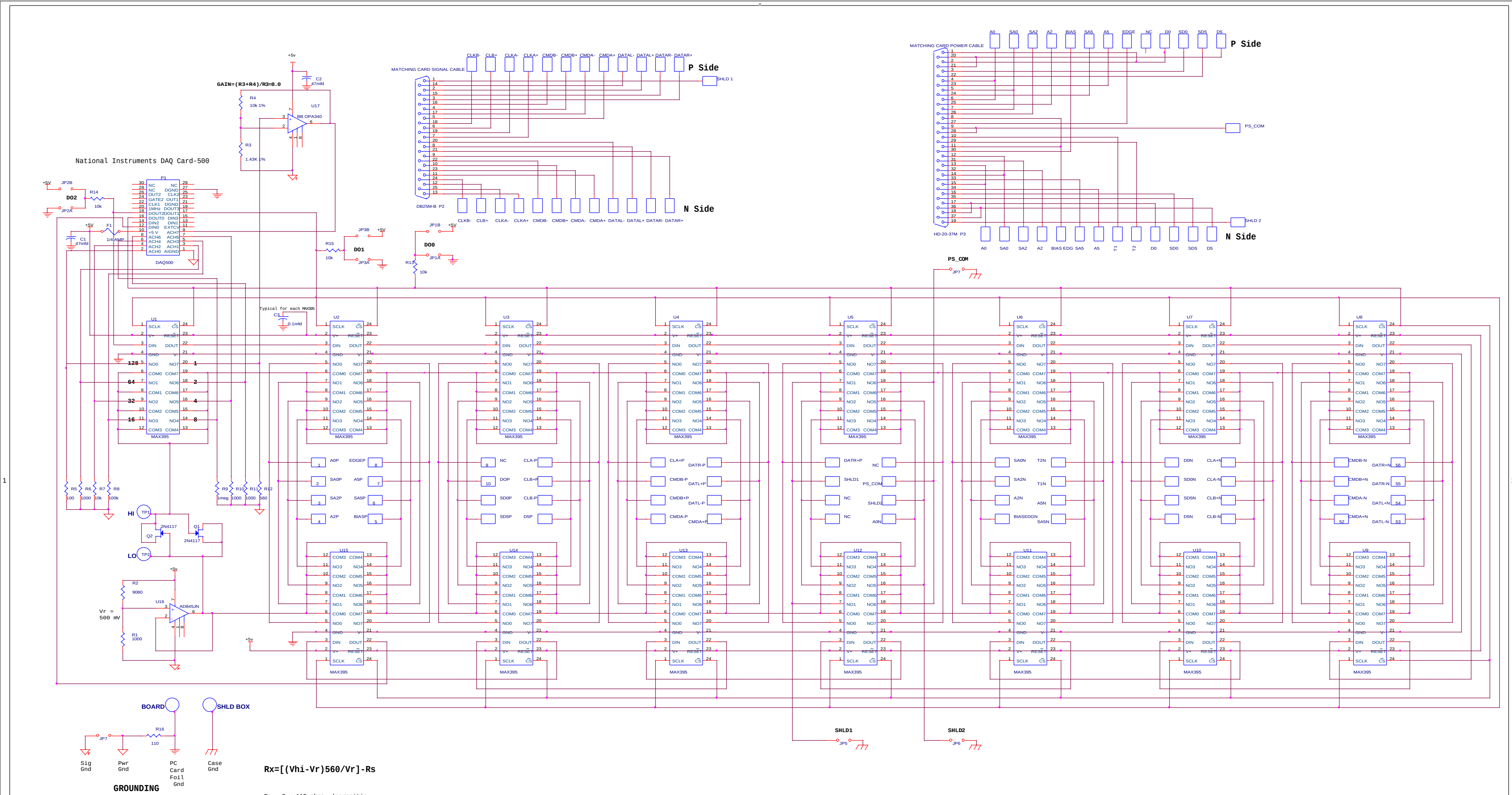

Rx=[(Vhi-Vr)560/Vr]-Rs

Rs = 2 x 115 ohms (parasitic switch resistance)

MAX395 INTERFACE DATA:

While the CS\ is low DIN is clocked into the Analog Switch register on the rising edge of the SCLK. When CS\ is brought high the data is latched internaly and the addressed analog switches are closed (1=closure). With CS\ high the SCLK no longer has any effect. The first data bit clocked in resides in the D0 register, it then moves to the D1 register with subsequent SCLK transitions.

BIT STREAM:

A total of 15*8=120 bits comprise the switching matrix setup word. The first bit out is U15-D7 with the last bit U1-D0. EXAMPLE: To carry out a test between T1N and T2N using the 10kohm load resistor the address in HEX is 04 00 00 00 00 00 40 00 00 00 00 80 00 00 00 00. The last 8 bit word (ie #04) sets up U1 for the 10k resistor and U6-NO6 with the #40 word and U11-NO7 is addressed with the #80 word. The DAQ500 A/D channel ADCH2 must be set up sperately.

BABAR CABLE TESTER 1
SCHEMATIC3
C:\ORCADWIN\CAPTURE\BABAR1\JUNPER2.DSN

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